# Babada Graphics Spedition.

#### Package Integrator & Sketch Router/Planner Board Centric Process

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## What are the problems with planning of DDR routing

- Planning of DDR routing from Package die to PCB Dimms is very time consuming.
- Many iterations may happen during pathfinding and beyond
- Routing of nets can be a challenge if placement of via farms and LGA pins is not optimal
- Routing proximity of byte lanes to each other is not preferred on back side (after core layers) routing (HLDRC)



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Current manual method of DDR Route planning using user layer graphics to determine layer and byte lane planning used on KNH





xpedition.

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### Unravel of via farms north before and after unravel





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## Process for creating and configuring the PCB and Package

- Generate symbol pin list from native CAD tool to create parts
  - Simplifies traditional board translation
- Import text file into XPI when adding part(s)
  - One spreadsheet with more data is good
  - Automation is useful when creating parts
  - Create via farm with multiple ILNs
  - Set swap regions
  - Setting pin groups and colors is helpful

#### **x**pedition

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# TCL Script for adding PCB database using symbol pin list generated from PCB Layout

This set of files need to be unzipped in the directory C:\temp\_XPI\Intel. Then you can open XPI and run the following command in the console (close the initial create/open dialog form). source C:\\temp\_XPI\\Intel\XPI\_Intel\_File\_KNH2\_PCB\\KNH\_xPI\_Commands.tcl



This will open a new KNH project. Adding the Design PCB. Read the KNH BGA and Conn288 devices and signal files. It finishes by doing Sync FE Design. At this point the script is done. These are the steps I did to complete the design and sync the layout.

•Select Device KNH\_BGA and run Edit >Buses > Autodetect Buses

•Select Device CONN288\_J1 and run Edit >Buses > Autodetect BusesSelect Design PCB and run Export > Connectivity to Layout (this will invoke the layout tool

1.Select the PCB.prj file. Form Next

2.Design Technology: Package, Template: Package Design 8 Layer Template. Form Finish then Close

3.Xpedition will Invoke

4.Copy the C:\temp\_XPI\Intel\XPI\_Intel\_File\_KNH2\_PCB \place.txt file into directory C:\temp\_XPI\Intel\KNH\PCB\PCB

5.Run FA

6.Run keyin "pr -file=place.txt"

7. Grow the Board Outline and Route Border

8.Save design and exit Xpedition

•In xPI run Import > Layout



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## Results of TCL Script to build PCB Database

Velue	▲ KHH2_MASTER_0503 □ 00 DDR3_1 □ 00 LGA_U110 □	Ø × Device		# X Pedroups	B x Objects Signals System
	M_CPU1_OG_[D[]*,M_CPU1_OH_[D[]*,M_CPU1_OG_[D[]*, Functional Signal (M_CPU1_OH3_[ HDL Name Instance Level Net	Instance		A Group name/ Type Including regex Excluding regex Included Excluded Punctional SL	Graphics     Device Pattern Display
	M_CPUL_CH3_DQ<0> M_CPU1_CH3_DQ<0> M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_DQ<0>     M_CPU1_CH3_D	Autom A		© CH4 AD10 AD2 AV4 © CH5 A10 A12 A81	
	M_07UL_08_00<7>     M_07UL_08_00<7>     M_07UL_08_00<7>     M_07UL_08_00<7>     M_07UL_08_00<7>	E Autom		UIIItat - Notepad	a B 11
	► M_07UL_00_DQ <d> M_07UL_00_DQ<d> M_07UL_00_DQ<d></d></d></d>	E Autom 7 .75 73 71 69 67	55 63 61 50 57 55 63 51 45 47 45   43 41 79 37 25 33 31 29 27 25 23 21 11 17	15 12 File Edit Format View Help 1010.44 x8643647 5 SKTPP, "XNH 200 EXT 1 864-0HPTY TBD" 017N209K12PHC19.6791.45.2377.36.6x0	
	M_000_00_004>     M_000_00_004>     M_000_00_004>     M_000_00_004>     M_000_00_004>	E Autom		U110, A6, X86A1647, 5, SKTPP, *KHL, 2CD, EXT, 3, B6A-EMPTY, TB0*, 017/2009KC17PVC19, 6223, 85, 7377, 36, EV, CPUL, J6M3_VIEw-0 U110, A6, X86A1647, 5, SKTPP, *KHL, 2CD, EXT, 3, B6A-EMPTY, TB0*, 017/2009KC17PVC19, 6156, 25, 2377, 36, EAD	> <u> </u>
	▶ M_CPUL_OB_DQ<6> M_CPUL_OB_DQ<6> M_CPUL_OB_DQ<6>	Autom		U10.412.x86a3647_5_SKTPP, "KH_2CD_LXT_3_BGA-BMPTY, TBD , 017X209K17MK19, 0086.05, 2377.36, M_CPU1_CH5_DQ<1> U10.412.x86a3647_5_SKTPP, "KH_2CD_LXT_3_BGA-BMPTY, TBD , 017X209K17MK19, 0082.05, 2377.36, M_CPU1_CH5_DQ<1> U10.414.x8Ga1647_5_SKTPP, "KH_2CD_LXT_3_BGA-BMPTY, TBD , 017X209K17MK19, 0082.05, 2377.36, M_CPU1_CH5_DQ<1>	
	M_0701_08_0Q<>     M_0701_	E Autom		U110.AL6.X86A1647_5_SKTPP, 'KAN_2CD_EXT_3_8GA-EMPTY_TBD', 017X209HC17PHC19, 5885.86, 2377.36, A_RFID_CPU0_EXT_AN U110.A24_X86A3647_5_SKTPP, 'KAN_2CD_EXT_3_8GA-EMPTY_TBD', 017X209HC17PHC19, 5615.46, 2377.36, GAD U110.A24_X86A3647_5_SKTPP, 'KAN_2CD_EXT_3_8GA-EMPTY_TBD', 017X209HC17PHC19, 5515.46, 2377.36, GAD	NT_OP
	► M_CPUL_OR_DQ<11> M_CPUL_OR_DQ<11> M_CPUL_OR_DQ<11>	E Autom		U110, A26, X86A3647_3_SKTPP, "KNH_2CD_EXT_3_86A-DHPTY, TBD", 017X209KC17PKC19, 5480, 27, 2177, 16, 0A0 U110, A10, X86A3647_5_SKTPP, "KNH_2CD_EXT_3_86A-DHPTY, TBD", 017X209KC17PKC19, 5412, 67, 2177, 16, PV_VCC1NL	
	M_090L08_00(12) M_090L08_00(12) M_090L08_00(12)      M_090L08_00(12) M_090L08_00(12)	El Autom		U110.A36.XBGA3647_5_SKTPP, 'KNK_2CD_EXT_3_BGA-LMPTY, TBD ',017x209KL7PKL19, 5274, 73, 50, PV CC1NL U110.A36,XBGA3647_5_SKTPP, 'KNK_2CD_EXT_3_BGA-LMPTY, TBD ',017x209KL7PKL19, 5274, 73, 76, PV_VCC1NL	
	M_GPUL_GR_DQ<14> M_GPUL_GR_DQ<14> M_GPUL_GR_DQ<14>     M_GPUL_GR_DQ<15> M_GPUL_GR_DQ<15>	Autom		ULID_A38_X8GA3647SXTPP, "KNH_2CD_EXTBGA-EMPTY, TBD", 017X205MC179MC19, 5142_27, 2377, 36, 6NO ULID_A40,X8GA3647_5_SKTPP, "KNH_2CD_EXTBGA-EMPTY, TBD", 017X205MC179MC19, 5074.68, 2377, 36, PV_VCCTML ULID_A42_X8GA3647_5_SKTPP, "KNH_2CD_EXTBGA-EMPTY, TBD", 017X205MC179MC19, 5077, 06, PV_VCCTML ULID_A42_X8GA3647_5_SKTPP, "KNH_2CD_EXTBGA-EMPTY, TBD", 017X205MC179MC19, 5077, 06, PV_VCCTML	
	M_CPUL_OR_DQS_DP<0>_MM_CPUL_OR_DQS_DP<0>_MM_CPUL_OR_DQS_DP<0>_M_CPUL_OR_DQS_DP<0>_M_CPUL_OR_DQS_DP<0>_M_CPUL_OR_DQSD>_M_CPUL_OR_DQS	El Autom		U110, AA2, XBGA1647_5_SKTPP, "KNH_2CD_EXT_2_BGA-DMPTY, TBD", C17PMC19, 6359, 05, 2767, 16, GAD U110, AA4, XBGA3647_5_SKTPP, "KNH_2CD_EXT_2_BGA-DMPTY, TBD", C17PMC19, 6259, 45, 2767, 36, GAD	
	M_CPUL_OR_DQ <> M_CPUL_OR_DQ <> M_CPUL_OR_DQ <> M_CPUL_OR_DQ <>	E Autom		U110.AA8.xEGA3647_5_SKTPP, "KNH_2CD_EXT_3_EGA_EMPTY_TED", C17PWC19, 6136, 25, 2767, 36, CAD U110.AA10.xEGA3647_5_SKTPP, "KNH_2CD_EXT_3_EGA_EMPTY_TED", C17PWC19, 6088, 65, 2767, 36, GAD	
	M_GPU1_GH3_DQ<17> M_GPU1_GH3_DQ<17> M_GPU1_GH3_DQ<17>	E Autom		U110.AA16.xBGA3647_5_SKTPP, 'KML_CD_EXT_J_BGA-ENPTY, TB0', C17PMC19, 5953.46, 2767.36, GAD U110.AA16.xBGA3647_5_SKTPP, 'KML_CD_EXT_J_BGA-ENPTY, TB0', C17PMC19, 5885.86, 2767.36, GAD	
	M_0PUL_00_0Q<0>     M_0PUL_00_0Q<0     M_0PUL_000_0Q<0     M_0PUL_00_0Q<0     M_0PUL	E Autom		UL10_AAL8_XBGA1647_5_SKTPP_XKH_2CD_EXT_3_BGA-KMPTY_TBD*_CL7PWC19_5818_26_2767_36_0V UL10_AA20_XBGA3647_5_SKTPP_XKH_2CD_EXT_3_BGA-KMPTY_TBD*_CL7PWC19_5750_66_2767_36_0ND UL10_AA22_XMGA1647_5_SKTPP_XKH_2CD_EXT_3_BGA-KMPTY_TBD*_CL7PWC19_5681_06_2767_36_0ND	
OH XPI VO DOR 6556 PMT ROARD ALLEGRINT	▶ M_CPUL_GRE_DQ<23>         M_CPUL_GRE_DQ<23>         M_CPUL_GRE_DQ<23>           ▶ M_CPUL_GRE_DQ<22>         M_CPUL_GRE_DQ<22>         M_CPUL_GRE_DQ<22>	Autom Autom		U110, AA24, XBGA3647_5_XXTPP, "XM_2CD_XXT_1_BGA-EXPTY_TBD", (17PHC19, 5615, 46, 2767, 56, 0A0 U110, AA26, XBGA3647_5_XXTPP, "XM_2CD_XXT_1_BGA-EXPTY_TBD", (17PHC19, 5417, 56, 2767, 56, 786, 786, 786, 787, 780, 787, 787, 787, 787, 787, 787	
Definition Ref Des Pattern Interface Layer Side	M_07UL_00_0Q+22>     M_07UL_00_0Q+22>     M_07UL_00_0Q+22>     M_07UL_00_0Q+22>     M_07UL_00_0Q+22>	Autom		(110, M30, M6G, M67, S., SKTPP, "NNL, COLEXT, J., BGA-UPPTY, TBO: C. LTPMC19, M12, 67, 2767, 16, PV, ACCIM, U110, MA12, M6G, M647, S., SKTPP, "NNL, COLEXT, J., BGA-UPPTY, TBO: C. TPMC19, 5145, 67, 2767, 16, PV, ACCIM, U110, MA12, M6G, M647, S., SKTPP, "NNL, 2COLEXT, J., BGA-UPPTY, TBO: C. TPMC19, 5145, 67, 2767, 16, PV, ACCIM,	
d H_2 KVH_2CD_EX V110 Contact	► M_GPU_GR_DQ<65> M_GPU_GR_DQ<65> M_GPU_GR_DQ<65>	Autom 28888888		UL10, Ax36, MBAX9647_5_SKTPP, "DNH_ZCD_EXT_JEGA-ENPTY, TBD", CL7PHC19, 5277, 47, 7767, 56, 6AD UL10, Ax36, MBAX9647_5_SKTPP, "DNH_ZCD_EXT_JEGA-ENPTY, TBD", CL7PHC19, 5209, 87, 2767, 36, PV_VCC1NL UL10, Ax38, MBAX9647_5_SKTPP, "DNH_ZCD_EXT_JEGA-ENPTY, TBD", CL7PHC19, 5124, 77, 2767, 36, 6AD	
_M 307 P76x78_3647L A1 Contact Interface	M.Conf.Conf.Dot.261.062.06437	Autom		U110.AM40, NBGA1867SERTPP_TON_ZCD_IXT_J_BGA-EMPTY, TBD", C17PHC18, 5074, 68, 2767, 36, PV_VCCTNL U120.AM42, NBGA1867_5_SERTPP_TON_ZCD_EXT_J_BGA-EMPTY, TBD ", C17PHC18, 5007, 68, 2767, 36, PV_VCCTNL U120.AM42, NBGA1867_5_SERTPP_TON_ZCD_EXT_J_BGA-EMPTY, TBD ", C17PHC18, 5007, 68, 2767, 36, PV_VCCTNL U120.AM45, NBGA1867_5_SERTPP_TON_ZCD_EXT_J_BGA-EMPTY, TBD ", C17PHC18, 5007, 68, 2767, 36, PV_VCCTNL	
KH KRAGHTS_HBL U2 Contact R.N DDR_NORTH DDR_NORTH Contact	M_GPUL_GB_DQ<24> M_GPUL_GB_DQ<24> M_GPUL_GB_DQ<24>     M_GPUL_GB_DQ<24>     M_GPUL_GB_DQ<25>     M_GPUL_GB_DQ<25>     M_GPUL_GB_DQ<25>	Autom		UL10, AA48, NBGA1647, S. SKTPP, "UNL_2CD_EXT_J_BGA-DPPTY, TBD", CL7PPC19, 4744, 10, 2696, 49, PV_VCCINO UL10, AA50, NBGA1647, S. SKTPP, "UNL_2CD_EXT_J_BGA-DPPTY, TBD", CL7PPC19, 4744, 10, 2696, 49, 600 UL10, AA50, NBGA1647, S. SKTPP, "UNL_2CD_EXT_J_BGA-DPPTY, TBD", CL7PPC19, 4676, 51, 2696, 49, 600	
R3_3 DDR3_0 DDR3_3 Contact R3_2 DDR3_0 DDR3_2 Contact	M_CPU1_CH3_DQ<26> M_CPU1_CH3_DQ<26> M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_CPU1_CH3_DQ<26>     M_C	Autom Autom		U110.4A54, X86A3647, 5, SKTPP, "TML 2CD_EXT_J_8GA-EMPTY, TBD", CLTPMC19, 4541, 31, 2696, 49, GAD U110.4A54, X86A3647, 5, SKTPP, "TML 2CD_EXT_J_8GA-EMPTY, TBD", CLTPMC19, 4541, 31, 2696, 49, PK, VCCEND	
R3_1 DDR3_0 DDR3_1 Contact R3_0 DDR3_0 DDR3_0 Contact	M_CPUL_CR5_DQ<31> M_CPUL_CR5_DQ<31> M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31> M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_CR5_DQ<31>     M_CPUL_	Autom		Ville, AASB, 380A,5904, 2., 34FPP, TMU_KCLEXTLGAL-EMPTY, TBC7, C17PVC19, 4406, 11, 2696, 49, PV_VCC1N0 U130, AA60, 38643647_5_SKTPP, TMU_KCLEXTLGAL-EMPTY, TBC7, C17PVC19, 4388, 11, 2696, 49, GMD U130, AA60, 38643647_5_SKTPP, TMU_KCLEXTLGAL-EMPTY, TBC7, C17PVC19, 4270, 92, 2696, 49, GMD	
RD LU LGA_U110 U110 Contact	► M_07U_06_0Q<29> M_07U_06_0Q<29> M_07U_06_0Q<29>	Autom Baranas		UL10. AM64. HEGA1647.5. SKTPP, "TWH_2C0_KYT_J_EGA-EMPTY, TB0", CL799CL9, 4203, 12, 2466, 49, FE, CP00_PEL_BX, 0P-CD-UL10. AA66, R66A3647.5. SKTPP, "TWH_2C0_KYT_J_EGA-EMPTY, TB0", CL799CL9, 4335, 72, 2656, 49, 600 UL10. AA66, R66A3647.5. SKTPP, "TWH_2C0_KYT_J_EGA-EMPTY, TB0", CL799CL9, 4365, 12, 2466, 49, 600 UL10. AA66, R66A3647.5. SKTPP, "TWH_2C0_KYT_J_EGA-EMPTY, TB0", CL799CL9, 4365, 12, 2466, 49, 600	
NU_36 CONU_36 36 Contact NN 35 CONU_36 35 Contact	M_CPUL_CH3_DQ+28>     M_CPUL_CH3_DQ+28	E Autom		U110, A470, MBA3647, 5, SKTPP, "DNH, 2CD, EXT. 3, BGA-EXPTY, THD", C17PHC19, 4000, 52, 2696, 49, GAD U110, A472, MBA3647, 5, SKTPP, "DNH, 2CD, EXT. 3, BGA-EXPTY, THD", C17PHC19, 4000, 52, 2696, 49, GAD U110, A472, MBA3647, 5, SKTPP, "DNH, 2CD, EXT. 3, BGA-EXPTY, THD", C17PHC19, 4000, 52, 2696, 49, GAD	
NU_34 CONN_34 34 Contact	M_0PUL_043_DQ<27>     M_0PUL_043_DQ<27>     M_0PUL_043_DQ<27>     M_0PUL_043_DQ<27>     M_0PUL_043_DQ<26>     M_0PUL_043_DQ<36>	Autom		U110,AA76,X8GA3647_S_SKTPP, "KNH_2CD_EXT_3_BGA-ENPTY, TBD ",C17PHC19,3797.73,2696.49,GND	-
NH_12 CONH_12 12 Contact NH_CONH_11 12 Contact	M_GPUL_GR_00_33>     M_GPUL_GR_00_33>     M_GPUL_GR_00_33>     M_GPUL_GR_00_33>     M_GPUL_GR_00_34>      M_GPUL_GR_00_34>      M_GPUL_GR_00_34>      M	El Autom		88	
e come a come	M_07UL_00_00(33) M_07UL_00_00(33) M_07UL_00_00(33)	E Autom 08888888		88	
	M_090E_08_00(32)     M_090E_08_00(32)     M_090E_08_00(32)     M_090E_08_00(32)	E Autom		Device properties	
	M_OPUL_OR3_DQ<37>     M_OPUL_OR3_DQ<37>     M_OPUL_OR3_DQ<37>     M_OPUL_OR3_DQ<39>	Autom	Device properties		
	M_CPUL_CR3_DQS_DP<4>_MM_CPUL_CR3_DQS_DP<4>_MM_CPUL_CR3_DQS_DP<4>_M_CPUL_CR3_DQS_DR<4> M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQS_DP<13>M_CPUL_CR3_DQ	El Autom	Pages Spreadsheet pins data		
	M_0PUL_00_00_0449     M_0PUL_00_00449     M_0PUL_00_00449     M_0PUL_00_00449      M_0PUL_000_00449      M_0PUL_000_0044      M_0PUL_000_0044      M_0PUL_000_0044      M_0PUL_000_0044      M_0PUL_000_004      M_0PUL_000_004      M_0PUL_000_004      M_0PUL_000_004       M_0PUL_000_004      M_0PUL_0	E Autom	Get and		
	M_GPU1_GH3_DQ<42> M_GPU1_GH3_DQ<42> M_GPU1_GH3_DQ<42>	E Autom	Define parameters for spreadsheet die import. Spreadsheet file: 2:Wenter Design/XPTWNH XPT VX2_DDR. 0505/u110.bt		
	M_DPUL_DB_DQ+B> M_DPUL_DB_DQ+B> M_DPUL_DB_DQ+B>     M_DPUL_DB_DQ+B> M_DPUL_DB_DQ+B>	El Autom	Deer Propidies	Attributes:	
	M_07U1_040_0Q<46> M_07U1_040_0Q<46> M_07U1_040_0Q<46>     M_07U1_040_0Q<46>     M_07U1_040_0Q<46>	ET Autom ET Autom	Delimiter:	Property Column order     Pin Number 2	
	■ M_OPULOB_DQS_DP<14>_MM_OPULOB_DQS_DP<14>M_OPULOB_DQS_DP<14>M_OPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14 >MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14>MOPULOB_DQS_DP<14 >MOPULOB_DQS_DP<14 >	E Autom	Ziterestevel Unit: TH	X Coord 7	
	M_CPUL_CH3_DQS_DP <s>,M M_CPUL_CH3_DQS_DP<s>,M M_CPUL_CH3_DQS_DP<s>,M_CPUL_CH3_DQS_DN<s></s></s></s></s>	E Autom	the optimizer	Signal Type	
	M_GPUL_GR_DQ <si> M_GPUL_GR_DQ<si> M_GPUL_GR_DQ<si></si></si></si>	El Autom	Pod size: 20	Functional Signal 0 Signal Direction	
	M_GPU1_GR0_DQ <s2> M_GPU1_GR0_DQ<s2> M_GPU1_GR0_DQ<s2>     M_GPU1_GR0_DQ<s3>     M_G</s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s3></s2></s2></s2>	Autom	Flow Innore header	Instance Level Ne 9	
	M_0PUL_OB_0Q <sh> M_0PUL_OB_0Q<sh> M_0PUL_OB_0Q<sh>     M_0PUL_OB_0Q<sh>     M_0PUL_OB_0Q<sh>     M_0PUL_OB_0Q<sh>     M_0PUL_OB_0Q<sh m_0pul_ob_0<="" m_0pul_ob_0q<sh="" m_0q<sh="" td=""><td>E Autom</td><td>Contraining</td><td></td><td></td></sh></sh></sh></sh></sh></sh></sh>	E Autom	Contraining		
	I M. (PUL CH8, DQS, DF<15>, M., M. (PUL CH8, DQS, DF<15>, M. (PUL CH8, DQS, DF<15>, M. (PUL CH8, DQS, DF<15>, M. (PUL CH8, DQS, DH<15>)	E Autom	Mirror		
	M_CPUL_CHI_DQS_IP<6>_MM_CPUL_CHI_DQS_IP<6>_MM_CPUL_CHI_DQS_IP<6>_MM_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6>_M_CPUL_CHI_DQS_IP<6	E Autom	Advanced		
	M_GPUL_GR0_DQ<8b> M_GPUL_GR0_DQ<8b> M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b> M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b      M_GPUL_GR0_DQ<8b>     M_GPUL_GR0_DQ<8b      M_GPUL_	E Autom	File preview: U110,A4,XBGA3047_5_SKTPP, %XHL2CD_DIT_J_BGA-EMPTY,TBD*,017X205MC17PMC1	19,6291.45,2377.36,040	
	M_CPU1_CH8_DQ<6L> M_CPU1_CH8_DQ<6L> M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_CPU1_CH8_DQ<6L>     M_	Autom	U110,A6,XBGA3647_5_SKTPP, YXH_2CD_EXT_J_8GA-EMPTY,T80*,017X205MC17FMC1 U110,A8,XBGA3647_5_SKTPP, YXH_2CD_EXT_J_8GA-EMPTY,T80*,017X205MC17FMC1	19,6223.45,2377.36,EV_CPU1_HBM3_VEW<0> 19,6156.25,2177.36,640	
	M_CPUL_CHE_DQ<57>     M_CPUL_CHE_DQ<57     M_C	Autom	U10,A10,305A3047,5_SKTPP,10H_2C0_EKT_J_BGA-EMPTY,TBD*,017X20596(1799C U10,A12,XBGA3647,5_SKTPP,10H_2C0_EKT_J_BGA-EMPTY,TBD*,017X20596(1799C U10,A14,XBGA3647,5_SKTPP,10H_2C0_EXT_J_BGA-EMPTY,TBD*,017X20596(1799C U10,A14,XBGA3647,5_SKTPP,10H_2C0_EXT_J_BGA-EMPTY,TBD*,017X20596(1799C	L39/0908-03/247-30/m_5v/U_508_DQ 479 C19/601.052377.36/M_CPUL_DB5_DQ 41> T0 5053.46.277.36.0/m	
	M_07U_00_0Q<36> M_07U_00_0Q<36> M_07U_00_0Q<36>	E Autom	U110,A16.X86A3047_5_SKTPP_YMB_ZC0_EKT_J_86A-EMPTY_TBD*_017X265MC1796C U110,A16.X86A3047_5_SKTPP_YMB_ZC0_EKT_J_86A-EMPTY_TBD*_017X265MC1796C U110,A24.X86A3647_5_SKTPP_YMB_XC0_EXT_J_86A-EMPTY_TBD*_017X265MC1796C	C19,5815.86,2377.36.A.RFD_CFU0_EXT_ANT_DP 12,9515.46.2372.36.0x0 V	
	M_CPUL_G0_DQ M_CPUL_G0_QQ M_CPUL_G0_DQ M_CPUL_G0_DQ M_CPUL_G0_DQ M_CPUL_G0_DQ M_CPUL_G0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_CPUL_Q0_DQ M_Q0_DQ M_Q0_DQ M_Q0_DQ M_Q0_Q0	E Autom	The following two fields can be used to define regular expressions allowing to find Pow	wer and Ground nets in file. Such nets will be converted to signals of the appropriate type. If no regular expressions are defined only multipln nets will be	
	M_CPU1_CH3_DQ<68> M_CPU1_CH3_DQ<68> M_CPU1_CH3_DQ<68>     M_CPU1_CH3_DQ<68>     M_CPU1_CH3_DQ<68>     M_CPU1_CH3_DQ5_DP<7>     M_CPU1_CH3_DQ7<     M_CPU1_CH3_DQ7<	E Autom	recognized and Vidi type will be assumed.		
	M_CPU1_CHI_DQ (58)     M_CPU1_CHI_DQ (58	Autom	Ground net require expression: CND		
	M CPUL CHI DOS DP-8> M M CPUL CHI DOS DP-8> M M CPUL CHI DOS DP-8> M CPUL CHI DOS DN-8>	TT Autom *			<u>8</u>
• • • • • • • • • • • • • • • • • • •	All Assigned Unessigned	<			·
In BOARD ALLESSO/CONS 73 successfully loaded					
tion BOARD_ALLEDBO/CONN_J4 successfully loaded tion BOARD_ALLESBO/CONN_J5 successfully loaded					
tion BOARD_ALLESBO/CONS_36 successfully loaded tion BOARD_ALLESBO/LOA_UIID successfully loaded					
lan successfully loaded for document BOASD_ALLEGRO/LGA_U110 has been successfully opened.					
d signals to symbol with dragging				OK Cancel	gnals, 0 selected Online  Scheme: D
				and sector	



## Results of TCL Script to build PCB Database



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## PCB Parts

A1       Package       3826.29134       3365.66929       0       V         J1       Package       370.07992       1202.25984       180       V       1         J2       Package       740.07874       1202.25984       180       V       1         J3       Package       1110.07874       1202.25984       180       V       1         J4       Package       6755.07874       1202.25984       180       V       1         J4       Package       6755.07874       1202.25984       180       V       1         J5       Package       7125.07874       1202.25984       180       V       1         J6       Package       7495.07874       1202.25984       180       V       1	A1       Package       3826.2913       3356.6929       0       V         D1       Package       370.07992       1202.25984       180       V         D2       Package       740.07874       1202.25984       180       V       0         D3       Package       1110.07874       1202.25984       180       V       0         D4       Package       6755.07874       1202.25984       180       V       0         D5       Package       7125.07874       1202.25984       180       V       0         D5       Package       7125.07874       1202.25984       180       V       0         D6       Package       7495.07874       1202.25984       180       V       0	Instance name	Database type	Position X(th)	Position Y(th)	Angle Horizontal Flip	Visibility	Group		1
11       Package       370.07992       1202.25984       180       Image: Control of Contr	11       Package       370.07992       1202.25984       180       Image: Control of Contr	A1	Package	3826.29134	3365.66929	0	<b>V</b>			
12       Package       740.07874       1202.25984       180       Image: Control of Contr	12       Package       740.07874       1202.25984       180       Image: 1110.07874       Image: 11100.07874       Image: 1110.07874 <t< td=""><td>31</td><td>Package</td><td>370.07992</td><td>1202.25984</td><td>180</td><td><b>V</b></td><td></td><td></td><td></td></t<>	31	Package	370.07992	1202.25984	180	<b>V</b>			
33       Package       1110.07874       1202.25984       180       Image: Control of Cont	33       Package       1110.07874       1202.25984       180       Image:	32	Package	740.07874	1202.25984	180	<b>V</b>			
J4       Package       6755.07874       1202.25984       180       Image: Constraint of the constr	14       Package       6755.07874       1202.25984       180       Image: Control of Cont	J3	Package	1110.07874	1202.25984	180 📃	<b>V</b>			
J5       Package       7125.07874       1202.25984       180       Image: Constraint of the state	15       Package       7125.07874       1202.25984       180       Image: Constraint of the constr	34	Package	6755.07874	1202.25984	180	<b>V</b>			
16       Package       7495.07874       1202.25984       180       Image: Control of Cont	16 Package 7495.07874 1202.25984 180 ♥	35	Package	7125.07874	1202.25984	180 📃	<b>V</b>			-
	OK Apply Cancel	36	Package	7495.07874	1202.25984	180	<b>V</b>			-
	OK Apply Cancel									



## Core Via Farm(s) with ILN's attached to multiple Instances

B 5-	ð =									ViaFarm_MASTER_DDR_DQ_CH3	0_3.csv - Excel			
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؇ Format	Painter	5 1		<u> </u>					Formatting - Table -					*
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-	: 2	< 🗸	<i>f</i> <sub>X</sub> 1											
A	в	С	D	E	F	G		н	Ι	J	К	L	м	N
1 Di	a_175	10	DQ1	0	C	DQ345	5 M_	1_CPU1_CH3_DQ<5>	M_CPU1_CH3_DQ<13>	M_CPU1_CH3_DQ<21>	M_CPU1_CH3_DQ<29>			
2 Di	ia_175	ю	DQ2	0	588	3 DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
3 Di	ia_175	ю	DQ3	0	1764	1 DQ345	5 M_	1_CPU1_CH3_DQ<4>	M_CPU1_CH3_DQ<12>	M_CPU1_CH3_DQ<20>	M_CPU1_CH3_DQ<28>			
4 Di	a_175	ю	DQ4	0	2352	2 DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
5 Di	a_175	ю	DQ5	508	-294	1 DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
6 Di	a_175	ю	DQ6	508	882	2 DQ345	5 M_	1_CPU1_CH3_DQ<0>	M_CPU1_CH3_DQ<8>	M_CPU1_CH3_DQ<16>	M_CPU1_CH3_DQ<24>			
7 Di	a_175	ю	DQ7	508	1470	DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
8 Di	a_175	ю	DQ8	608.278	2471.896	5 DQ345	5 M_	1_CPU1_CH3_DQS_DP<9>	M_CPU1_CH3_DQS_DP<10>	M_CPU1_CH3_DQS_DP<11>	M_CPU1_CH3_DQS_DP<12>			
9 Di	ia_175	ю	DQ9	915.723	1938.104	1 DQ345	5 M_	1_CPU1_CH3_DQS_DN<9>	M_CPU1_CH3_DQS_DN<10>	M_CPU1_CH3_DQS_DN<11>	M_CPU1_CH3_DQS_DN<12>			
10 Di	ia_175	IO	DQ10	1016	C	DQ345	5 M_	1_CPU1_CH3_DQ<1>	M_CPU1_CH3_DQ<9>	M_CPU1_CH3_DQ<17>	M_CPU1_CH3_DQ<25>			
11 Di	ia_175	ю	DQ11	1016	588	3 DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
12 Di	ia_175	ю	DQ12	1524	-294	1 DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
13 Di	ia_175	ю	DQ13	1524	882	2 DQ345	5 M_	I_CPU1_CH3_DQ<7>	M_CPU1_CH3_DQ<15>	M_CPU1_CH3_DQ<23>	M_CPU1_CH3_DQ<31>			
14 Di	a_175	ю	DQ14	1524	1470	DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
15 Di	a_175	ю	DQ15	1624.278	2471.896	5 DQ345	5 M_	1_CPU1_CH3_DQS_DP<0>	M_CPU1_CH3_DQS_DP<1>	M_CPU1_CH3_DQS_DP<2>	M_CPU1_CH3_DQS_DP<3>			
16 Di	a_175	ю	DQ16	1931.723	1938.104	1 DQ345	5 M_	1_CPU1_CH3_DQS_DN<0>	M_CPU1_CH3_DQS_DN<1>	M_CPU1_CH3_DQS_DN<2>	M_CPU1_CH3_DQS_DN<3>			
17 Di	ia_175	ю	DQ17	2032	C	DQ345	5 M	I_CPU1_CH3_DQ<6>	M_CPU1_CH3_DQ<14>	M_CPU1_CH3_DQ<22>	M_CPU1_CH3_DQ<30>			
18 Di	a_175	ю	DQ18	2032	588	3 DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
19 Di	a_175	ю	DQ19	2540	-294	1 DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
20 Di	a_175	ю	DQ20	2540	882	2 DQ345	5 M	1_CPU1_CH3_DQ<2>	M_CPU1_CH3_DQ<10>	M_CPU1_CH3_DQ<18>	M_CPU1_CH3_DQ<26>			
21 Di	a_175	ю	DQ21	2540	1470	DQ345	5 (N	Net0)	(Net0)	(Net0)	(Net0)			
22 Di	a_175	ю	DQ22	2540	2646	5 DQ345	5 M_	I_CPU1_CH3_DQ<3>	M_CPU1_CH3_DQ<11>	M_CPU1_CH3_DQ<19>	M_CPU1_CH3_DQ<27>			

Could change IO to diff pair parent name, and include color, *possible swap code ILNs\** in this spreadsheet. Using one spreadsheet for both part creation and/or signal source would be useful. Also, the ability to use multiple ILN would be good when building part if possible.

#### **x**pedition



## **Building Via Farms**

1		? ×
	Device properties	
roject - [KNH_XPI_VX2_DDR_0516_PM] [KNH2_MASTER_050         nstance       Definition       Ref Des       Pattern         board       KNH2_CD_EX       U10       Contact         KNH2_M       KNH2_CD_EX       U10       Contact         WiaFar       ViaFarm_DDR       DDR3_0       Contact         WinFar       ViaFarm_DDR       DDR3_0       Contact         Image: Convolution of the state of the s	Image: Specific provide the specific provide specific provid	
x peditio	© 2014 Mentor Graphics Corp. Compan www.mentor.com	y Confidenti



## Multiple ILN's for multiple instances

iew Setup Assign Symbol Import Export Tools	Help			Xpedition Package I	ntegrator [KNH_XPI_VX2_DDR_0516	_PM*] [KNH2_MASTER_0503 : DI	DR3_0]			
2 <b>6 9 6 %</b> % % % % % %	• ~ • • • •				& <u>A</u> & A & A					Display Control
Value	SI	ignels			∂ × Pns		8 × Device			e x Objects Signals Si
	<u>_Fi</u>	Inctional Signal HDL Name	Instance Level Net	Instance Lev., Dir	Pin [1689]*,[1230*,22*,1,1[ Pin,1[35-7]*,) Name	Functional Signal Instance Level N	Net			A board     Visibility
		DQ1     DQ10     DQ10     DQ11	M_CPU1_CH3_DQ<1> (Me0)	Cyan In	1	DQ20 M_CPU1_CH3_D DQ20 M_CPU1_CH3_D DQ17 M_CPU1_CH3_D	N (3) / / / / / / / / / / / / / / / / / / /			J ✓ Name ₩ ✓ board_floor
		DQ12     DQ12     DQ13     DQ13	(Net0) M_CPU1_CH3_DQ<7>	Automatic In	12 # 16 16 13 # 15 15	0016 M_CPU1_CH3_D 0015 M_CPU1_CH3_D	DQS_DN<0> DQS_DP<0>			BOARD_ALLEGRO
		DQ14     DQ14     DQ15     DQ15	(Net0) M_CPU1_CH3_DQ5_DP<0>	Automatic In	14 # 13 13 15 # 10 10	0Q13 M_CPU1_CH3_D 0Q10 M_CPU1_CH3_D	φα>			Visibility
		<ul> <li>▶ 0Q16</li> <li>▶ 0Q17</li> <li>▶ 0Q17</li> </ul>	M_CPU1_CH0_DQ5_DN<0> M_CPU1_CH3_DQ<6>	Automatic In	16 # 9 9 17 # 8 8	DQ9 M_CPU1_CH3_D DQ8 M_CPU1_CH3_D	DQS_DN<9> DQS_DP<9>			board_alleg
		DQ18     DQ19     DQ19	(Net0) (Net0)	Automatic In Automatic In	18 # 6 6 19 # 3 3	0Q6 M_CPU1_CH3_D 0Q3 M_CPU1_CH3_D	xQ<0> xQ<4>			E ✓ CONN_J2 E ✓ CONN_J3
		► 0Q2 0Q2 ► 0Q20 0Q20 ► 0Q21 0Q21	(Nett) M_CPU1_CH3_DQ<2> (Nett)	Cyan In	20	ndi w"choi"chi"n	Act 1			■ CONN_J4 ■ CONN_J5
		► 0Q22 DQ22 ► 0Q3 DQ3	M_CPU1_CH3_DQ<3> M_CPU1_CH3_DQ<4>	Cyan In	22		/			■ ✓ CONN_J6 ■ ✓ LGA_U110
		DQ4     DQ4     DQ5     DQ5	(Net0) (Net0)	Automatic In	4 5					■ ♥ P76x78_364
		► 0Q6 0Q6 ► 0Q7 0Q7	M_CPU1_CH3_DQ<0> (Net0)	Cyan In Automatic In	6 7					Visibility 네 군 Name
		<ul> <li>bda</li> <li>bda</li> <li>bda</li> <li>bda</li> </ul>	M_CPU1_CH3_DQ5_DP<9> M_CPU1_CH3_DQ5_DN<9>	Automatic In In	9					■   DDR3_0 ■   DDR3_1
								$\square$	$\sim$	■ ✓ DDR3_2 ■ ✓ DDR3_3
										DDR_NOR
										KNIGHTS,     Ø     ✓ P76x78_36
				Device properties			? ×			
	Device pr	roperties								
X2_DDR_0516_PM*] [XNH2_MASTER_0503]	Pages	Spreadsheet signals data								
Definition Ref Des Patter	n Start	Define parameters for spreadsheet signal	mport.							
T_J_BGA-EMPTY,TBD KNH_2CD_EX U110 Contai _0503 1.01A P76x78.3647LA1 Contai	t User	Spreadsheet file: Z:\Mentor_Designs\XPDXNH	XPL VX2_DDR_0505(killH2_MASTER_0516\Output\VieFerm_MAS	TER_DDR_DQ_CH3_0_3.csv						
L_90_BC_A0_9967 KNIGHTS_HILL UZ Contai DDR_NORTH DDR_NORTH Contai	t Device	Ignore header								
DDR3_0 DDR3_3 Contai DDR3_0 DDR3_2 Contai DDR3_0 DDR3_1 Contai	d Coreadateet	Delimiter:	l.	·						
DDR3_0 DDR3_0 Contai	t in L Signats	Property Column order		Instance Name	ILN Column				$\sim$	
LO1A KNH2_MASTE P76x78_3647L Conter LGA_U110 U110 Conter CONN 16 35 Conter	tt ZSpreadsheet	Signal type Signal direction		4 K0H2_MASTER_0503/00R3_ 3 K0H2_MASTER_0503/00R3_ K0H2_MASTER_0503/00R3_			9			
CONN_35 35 Contai CONN_34 34 Contai	tt saw, Flow	DIFF parent nam Pin number		KNH2_MASTER_0503/DDR3_			11			
CONN_13 13 Contex CONN_32 12 Contex CONN 31 Contex	d Settings	Celor								
	10 Advanced									
	1.000									
		Data preview:	4 5 6 7	8 9	10 1	1	<u> </u>			
		1 1 Dis_175 10 2 2 Dis_175 10	0Q1 0 000 0Q2 0 588 00 002 1264 00	345         M_OPU1_OH3_DQ<5>         M_OPU1_           345         (Net0)         (Net0)	043_DQ<13> M_CPU1_CH3_DQ<21> // (Net0) ()	4_CPU1_CH3_D Net0)				
		4 4 Dia_175 10 5 5 5 Dia_175 10	0Q3 0 1700 0 0Q4 0 2352 0 005 508 -204 0	345 (Net0) (Net0) (Net0)	(Net0) (Net0)	Net0)		$\frown$		
		6 6 0ia_175 10 7 7 0ia_175 10	DQ6 508 882 DQ DQ7 508 1470 DQ	345 M_OPU1_OH3_DQ<0> M_OPU1_ 345 (Net0) (Net0)	0H3_DQ<8> M_CPU1_CH3_DQ<16> (Net0) (	(_CPU1_CH3_D Net0)				
		8 8 0ia_175 10 9 9 0ia_175 10	0Q8 608.278 2471.896 00 0Q9 915.723 1938.104 00	345         M_CPU1_CH3_DQ5_DF<9>         M_CPU1_           345         M_CPU1_CH3_DQ5_DN<9>         M_CPU1_	H3_DQ5_DP<10 M_CPU1_CH3_DQ5_DP<11> // H3_DQ5_DN<10 M_CPU1_CH3_DQ5_DN<11> //	(_CPU1_CH3_D (_CPU1_CH3_D				
		10 10 Dia_175 ED 11 11 Dia_175 ED 13 11 Dia_175 ED	0Q10 1016 000 0Q11 1016 588 00 0Q12 1524 304 00	MOPU1OH3_DQ<1>         MOPU1           345         (Net0)         (Net0)           M5         (Net0)         (Net0)	M_DQ<9> M_CPU1_CH3_DQ<17> (Net0) (	Net0)				
		13 13 Dia_175 10 14 14 Dia_175 10	DQ13 1524 882 DQ DQ14 1524 1470 DQ	345 M_CPU1_CH3_DQ<7> M_CPU1_ 345 (Net0) (Net0)	(Net0) (N	4_CPU1_CH3_D Net0)				
		15 15 Dis 175 10	0015 1624 378 3471 896 00	M CRUI CHR DOS DE/DS M CRUI	WA DOS DROT M CRID CHA DOS DROT	CRII. CHI. D	×			
	-									
						ОК С	Cancel			
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	>	All Assigned Unassigned			<		> <			>
og Level: All messages 🔹 🥅 🚓 🕈 🕇										
ment board/KNM 2CD EXT J BGA-EMPTY, TBD has been t Z:\\Mentor Designs\\XPI\\KNM XPI VX2 DDR 0505	successfully opened. \\PINGROUP.xml									
ties -key BOARD_ALLEGRO/LGA_U110 -flightlines O ties -key BOARD_ALLEGRO/P76x78_3647L_01A -fligh	tlines ON									
ASTER_0503/DDR3_0										
									xy: 1264.07941 7567.16031 da	xdy: -480.52335 -77.92272 th Online 🖲 Scheme: Dx
									014 Mantan Cranking Co	Commence Concile
								C 4	UIA MERILOI Graphics CO	rp. Company confide



## Defining DDR BYTE Lane pin groups

Name Value	Signals	ð x Pins	6 × Device
Type Food	Functional Signal HOL Name Instance Level Net Instance Lev	Dir         Pin         Number /         Name         Functional Signal         Instance Level Net	·*
rms [100	M_CPU1_CH3_DQ<0>         M_CPU1_CH3_DQ<0>         M_CPU1_CH3_DQ<0>         Cyan           M_CPU1_CH3_DQ<2>         M_CPU1_CH3_DQ<2>         M_CPU1_CH3_DQ<2>         Cyan	In TI ^ @ Y1 Y1 In W6 @ W86 W86	
	▶ M_CPU1_CH3_DQ<1>         M_CPU1_CH3_DQ<1>         M_CPU1_CH3_DQ<1>         Cyan           ■ > M_CPU1_CH3_DQ5_DP<0>_M	In R1 © W84 W84 In U1 © W82 W82	
	M_CPU1_CH3_DQ <s>         M_CPU1_CH3_DQ<s>         M_CPU1_CH3_DQ<s>         CPU1_CH3_DQ<s>           M_CPU1_CH3_DQ&lt;4&gt;         M_CPU1_CH3_DQ&lt;4&gt;         M_CPU1_CH3_DQ&lt;4&gt;         Gypt</s></s></s></s>	In W2	66858483828160797877767574737271706564556655645382616059565756555453525150494847464544 43424140393837363534332231302928272625242322212019181716151413121110 9 8 7 6 5 4 3 2
	M_CPU1_CH3_DQ<6>         M_CPU1_CH3_DQ<6>         M_CPU1_CH3_DQ<6>         Cypn           M_CPU1_CH3_DQ<7>         M_CPU1_CH3_DQ<7>         M_CPU1_CH3_DQ<7>         Cypn	In 17      W76 W76     W74     W74	
	▶         M_CPU1_CH3_DQ<3>         M_CPU1_CH3_DQ<3>         ■ Cymn           ■         >         M_CPU1_CH3_DQS_DP<9>_M         M_CPU1_CH3_DQS_DP<9>_M         M_CPU1_CH3_DQS_DP<9>_M	In V7 • W72 W72 In U8 • W70 W70	
	M_CPU1_CH3_DQ<10>         M_CPU1_CH3_DQ<10>         M_CPU1_CH3_DQ<10>         Cyan           M_CPU1_CH3_DQ<11>         M_CPU1_CH3_DQ<11>         M_CPU1_CH3_DQ<11>         Cyan	In KG © W68 W68 In K2 © W66 W66	
	M_CPU1_CH3_DQ<12>         M_CPU1_CH3_DQ<12>         Cyan           M_CPU1_CH3_DQ<13>         M_CPU1_CH3_DQ<13>         M_CPU1_CH3_DQ<13>	In MS @ W62 W62	
	M_CPUI_CH3_DQ<14>         M_CPUI_CH3_DQ<14>         M_CPUI_CH3_DQ<15>         Cyan           M_CPUI_CH3_DQ<15>         M_CPUI_CH3_DQ<15>         M_CPUI_CH3_DQ<15>         Cyan	In H3	
	M_CPU1_Cd3_DQ <b>         M_CPU1_Cd3_DQ<b>         M_CPU1_Cd3_DQ<b>         Cyan           M_CPU1_Cd3_DQS_DP&lt;1&gt;         M_CPU1_Cd3_DQS_DP&lt;1&gt;         M_CPU1_Cd3_DQS_DP&lt;1&gt;         M_CPU1_Cd3_DQS_DP&lt;1&gt;</b></b></b>	In 10 VIS6 VIS6 In 14 VIS6 VIS6	
	M_CPU_CH3_DQS_DN<1> M_CPU_CH3_DQS_DN<1> M_CPU_CH3_DQS_DN<1> M_CPU_CH3_DQS_DN<1> M_CPU_CH3_DQS_DN<1> M_CPU_CH3_DQS_DN<1> M_CPU_CH3_DQS_DN<10 M_CPU_CH3_DDS_DN<10     M_CPU	In KS © W50 W50	
	M_CPU1_CH3_DQ5_DP<10> M_CPU1_CH3_DQ5_DP<10> M_CPU1_CH3_DQ5_DP<10> Automatic     M_CPU1_CH3_DQ5_DP<10> M_CPU1_CH3_DQ5_DP<10> Curve	Dn 34 @ W46 W46	
Product, Data we loss one sets and funct literee areas	M_CPU1_CH3_DQ<17> M_CPU1_CH3_DQ<17> M_CPU1_CH3_DQ<17> Cym     M_CPU1_CH3_DQ<17> Cym     M_CPU1_CH3_DQ<18> M_CPU1_CH3_DQ<18> Cym	In W2  V40 W40 In M4 V38	🗉 elabelalalala, labelalalalalalalala, mananananana, entertetara.
Instance Definition Ref Des Pattern 1	M CPUI_CH3_DQ<19>     M CPUI_CH3_DQ<19>     M CPUI_CH3_DQ<19>     M CPUI_CH3_DQ<19>     M CPUI_CH3_DQ<20>     M CPUI_CH3_DQ<20	In TS	🗱 HARABARAAAAAAAAAAAAAAAAAAAAAAAA BAAAAAAAA
board     KNH_2 KNH_2CD_EX U110     Contect	M_CPUI_CH3_DQ<21>         M_CPUI_CH3_DQ<21>         M_CPUI_CH3_DQ<21>         CPUI_CH3_DQ<21>           > M_CPUI_CH3_DQ<22>         M_CPUI_CH3_DQ<22>         M_CPUI_CH3_DQ<22>         M_CPUI_CH3_DQ<22>	In T1	
KNR2_M     P76x78. P76x78_3647L A1 Contect IF     KNR2H KNR2HTS HILL U2 Contect	terfac M_CPU1_CH3_DQ<23> M_CPU1_CH3_DQ<23> M_CPU1_CH3_DQ<23> M_CPU1_CH3_DQ<23> Cyan	In W W28 W28 In T3 W26 W26	
DDR.N DDR.NORTH DDR.NORTH Contact DDR3_3 DDR3_0 DDR3_3 Contact	M_CPU1_CH3_DQS_DP<11> M_CPU1_CH3_DQS_DP<11> M_CPU1_CH3_DQS_DP<11> Automatic     M_CPU1_CH3_DQS_DN<2> M_CPU1_CH3_DQS_DN<2> M_CPU1_CH3_DQS_DN<2> Automatic	In U4 © W24 W24 In V3 © W22 W22	
DDR3_2 DDR3_0 DDR3_2 Contact DDR3_1 DDR3_0 DDR3_1 Contact	M_CPU1_CH3_DQS_DP<2>         M_CPU1_CH3_DQS_DP<2>         M_CPU1_CH3_DQS_DP<2>         Automatic           M_CPU1_CH3_DQ<25>         M_CPU1_CH3_DQ<25>         M_CPU1_CH3_DQ<25>         Cyan	In U2	
BORD_0 DDR3_0 DDR3_0 Contact	M_CPU1_CH3_DQ<26>         M_CPU1_CH3_DQ<26>         M_CPU1_CH3_DQ<26>         Cyan           M_CPU1_CH3_DQ<27>         M_CPU1_CH3_DQ<27>         M_CPU1_CH3_DQ<27>         Cyan	In AY. # W16 W16PU1_CH4_DQ <s> M_CPU1_CH4_DQ<s> In AW # W14 W14PU1_CH4_DQ&lt;2&gt; M_CPU1_CH4_DQ&lt;2&gt;</s></s>	
CONV_36 CONV_36 36 Contact     CONV_35 CONV_35 Contact     CONV_35 CONV_35 Contact	M_CPU1_CH3_DQ<28>         M_CPU1_CH3_DQ<28>         M_CPU1_CH3_DQ<28>         Gym           M_CPU1_CH3_DQ<29>         M_CPU1_CH3_DQ<29>         M_CPU1_CH3_DQ<29>         Gym	In AV • W12 W12 In AY • W10 W10PU1_CH3_DQ <s> M_CPU1_CH3_DQ<s></s></s>	
CONN_H CONN_H H Contect CONN_J3 CONN_J3 J3 Contect	M_CPU1_CH3_DQ<30>         M_CPU1_CH3_DQ<30>         M_CPU1_CH3_DQ<30>         CPU1_CH3_DQ<30>           M_CPU1_CH3_DQ<31>         M_CPU1_CH3_DQ<31>         M_CPU1_CH3_DQ<31>         CH3_DQ<31>	In AU W8 W8PU1_CH3_DQ<2> M_CPU1_CH3_DQ<2> In AT W6 W6	
CONN_32_CONN_32 J2 Contact	M_CPUI_CH3_DQS_DH<22     M_CPUI_CH3_DQS_DH<12     M_CPUI_CH3_DQS_DH<12     M_CPUI_CH3_DQS_DH<2     M_CPUI_CH3_DQS_DH<3	In AV W2 W401_CH3_DQ4235 M_CH01_CH3_DQ4255 In AV W2 W2U1_CH3_DQ4175 M_CH01_CH3_DQ4175	🚾 📓 * 39339339339339333
	M_CPU_CH3_DQS_DP+32     M_CPU_CH3_DQS_DP+3	In AV © V83 V83 In AV © V83 V83	
	M_CPU1_CH3_DQ<32> M_CPU1_CH3_DQ<32> M_CPU1_CH3_DQ<32> Automatic     M_CPU1_CH3_DQ<32> M_CPU1_CH3_DQ<33> M_CPU1_CH3_	In DK V79 V79 In DK V77 V77	- HEREBERERE - HEREBERERERE
	▶ M_CPU1_OR_DQ<34>         M_CPU1_OR_DQ<34>         M_CPU1_OR_DQ<34>         Automatic           ▶ M_CPU1_OR_DQ<35>         M_CPU1_OR_DQ<35>         M_CPU1_OR_DQ<35>         Automatic	In DG V75 V75 In DH V73 V73	
	▶ M_CPU1_CH3_DQ<36>         M_CPU1_CH3_DQ<36>         ▲ Automatic           ▶ M_CPU1_CH3_DQ<37>         M_CPU1_CH3_DQ<37>         M_CPU1_CH3_DQ<37>         Automatic	In DG	
	M_CPU1_CH3_DQ<38>         M_CPU1_CH3_DQ<38>         M_CPU1_CH3_DQ<38>         Automatic           M_CPU1_CH3_DQ<39>         M_CPU1_CH3_DQ<39>         M_CPU1_CH3_DQ<39>         Automatic	In DK © V67 V67 In DU © V65 V65	👅 HARABAAAAAAAAAA
	M_CPU1_CH3_DQS_DN<13> M_CPU1_CH3_DQS_DN<13> M_CPU1_CH3_DQS_DN<13> Automatic     M_CPU1_CH3_DQS_DN<4> M_CPU1_CH3_DQS_DN<4> M_CPU1_CH3_DQS_DN<4> Automatic	In DK 🛛 V63 V63 In DH 🖉 V61 V61	📲 HEREEHET EREREEKEN
	M_CPU1_CH3_DQS_DP<13> M_CPU1_CH3_DQS_DP<13> M_CPU1_CH3_DQS_DP<13> Automatic     M_CPU1_CH3_DQS_DP<4> M_CPU1_CH3_DQS_DP<4> Automatic     M_CPU1_CH3_DQS_DP<4> Automatic	In D16	
	M_CPU1_CH3_DQ<40>         M_CPU1_CH3_DQ<40>         M_CPU1_CH3_DQ<40>         Automatic           M_CPU1_CH3_DQ<41>         M_CPU1_CH3_DQ<41>         M_CPU1_CH3_DQ<41>         Automatic	In DK V55 V35 In DL V53 V53	
	M_CPU1_O3_DQ<42> M_CPU1_C13_DQ<42> M_CPU1_C13_DQ<42> M_CPU1_C03_DQ<42> Automatic     M_CPU1_O3_DQ<43> M_CPU1_C13_DQ<43> M_CPU1_C13_DQ<43> Automatic	In OC V31 V31 In OH V49 V49	
	M_CPU_CH3_0Q+45> M_CPU_CH3_0Q+45> M_CPU_CH3_0Q+45> Automatic     M_CPU_CH3_0Q+45> M_CPU_CH3_0Q+45> M_CPU_CH3_0Q+45> Automatic	In DG © V45 V45	
	M_CPU_C03_DQS_DN <s> M_CPU_C03_DQS_DN<s> M_CPU_C03_DQS_DN<s automatic="" m_cpu_c03_dqs_dn<s=""> M_CPU_C03_DQS_DN<s automatic="" m_cpu_c03_dqs_dn<s=""> M_CPU_C03_DQS_DN<s automatic<="" td=""><td>In DJ</td><td></td></s></s></s></s></s>	In DJ	
	M_CPU1_CH3_DQ5_DN<14>     M_CPU1_CH3_DQ5_DN<14	In D1 • V37 V37 In DX • V35 V35	
	M_CPU1_CH3_DQS_DP <s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> Automatic     M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> Automatic     M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s>     M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s>     M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3_DQS_DP<s> M_CPU1_CH3</s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s></s>	In 04 @ V33 V33 In 08 @ V31 V31	
	M_CPU1_CH3_DQS_DP<15>     M_CPU1_CH3_DQS_DP<15>     M_CPU1_CH3_DQS_DP<15>     M_CPU1_CH3_DQS_DP<15>     M_CPU1_CH3_DQS_DN<6>     M_CPU1_CH3_D	In DL	
	M_CPUI_CH3_DQ<48>         M_CPUI_CH3_DQ<48>         M_LCPUI_CH3_DQ<48>         Automatic           M_CPUI_CH3_DQ<54>         M_CPUI_CH3_DQ<54>         M_CPUI_CH3_DQ<54>         Automatic	In DM © V25 V25 In DM © V23 V23	
	M_CPU1_CH3_DQ<49>         M_CPU1_CH3_DQ<49>         M_CPU1_CH3_DQ<49>         Automatic           M_CPU1_CH3_DQ<50>         M_CPU1_CH3_DQ<50>         M_CPU1_CH3_DQ<50>         Automatic	In DN © V21 V21 In DJ © V19 V19	868564838281807578777875747574757475747574757475747574
	M_CPU1_CH3_DQ <s2> M_CPU1_CH3_DQ<s2> M_CPU1_CH3_DQ<s2> M_CPU1_CH3_DQ<s2> Automatic     M_CPU1_CH3_DQS_DN&lt;1S&gt; M_CPU1_CH3_DQS_DN&lt;1S&gt; Automatic</s2></s2></s2></s2>	In DJ. V17 V17PU1_CH4_DQ<4> M_CPU1_CH4_DQ<4> In DK V15 V15H4_DQS_DN<0> M_CPU1_CH4_DQS_DN<0>	
	M_CPUI_CH3_DQ <s3> M_CPUI_CH3_DQ<s3> M_CPUI_CH3_DQ<s3> ALtomatic     M_CPUI_CH3_DQ<s5> M_CPUI_CH3_DQ<s5> M_CPUI_CH3_DQ<s5> ALtomatic</s5></s5></s5></s3></s3></s3>	In DK V13 V13PU1_CH4_DQ<3> M_CPU1_CH4_DQ<3> In DN V11 V11PU1_CH3_DQ<4> M_CPU1_CH3_DQ<4>	
	M_CPU1_CH3_DQS_DP<6> M_CPU1_CH3_DQS_DP<6> M_CPU1_CH3_DQS_DP<6> Automatic     M_CPU1_CH3_DQ<61> M_CPU1_CH3_DQ<61> M_CPU1_CH3_DQ<61> Automatic	In DL V9 V9H3_DQS_DN<0> M_CPU1_CH3_DQS_DN<0> In DD V II V7 V7PU1_CH3_DQ<3> M_CPU1_CH3_DQ<3>	
K II	> All Assigned Unassigned	VS VSCHU1_CHB_0Q<22> M_CHU1_CHB_0Q<22>	
Console			

entor

## Assign Crankshaft Vias on Via Farms

Create and assign via crankshafts with net adoption from selected pins or existing net objects in added crankshaft via location.

- 1. Via crankshaft toolbar and file control
- 2. Extract via crankshaft from selected
- 3. Interactive build via crankshaft
- 4. Via crankshaft Table
- 5. Dynamic and menu placement control

#### **x**pedition



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## PCB with package LGA and Board LGA View per Byte lane







#### Die and PCB Floorplan in Floorplan XPI view and PCB View



#### **PCB Before and After Unravel**



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#### xPI and xPCB Sketch Planner view



## PCB view with Package Floor plan with trunk routing



Men

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## Package Integrator Demo

## Sketch Router/Planner/Trunk routing demo



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