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Package Integrator & Sketch Router/Planner Board Centric Process

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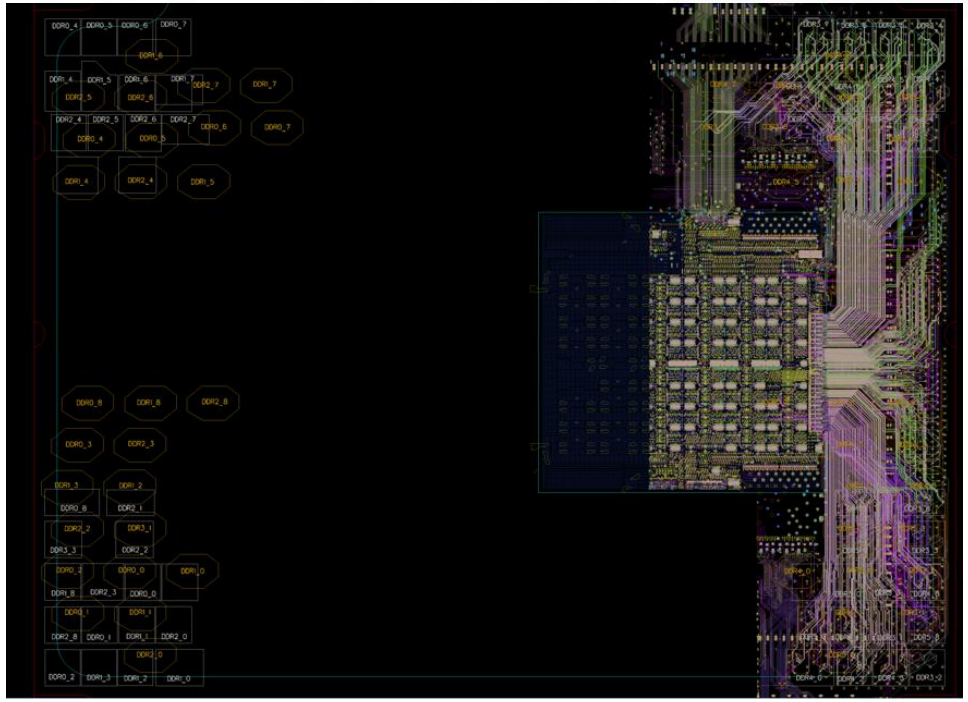
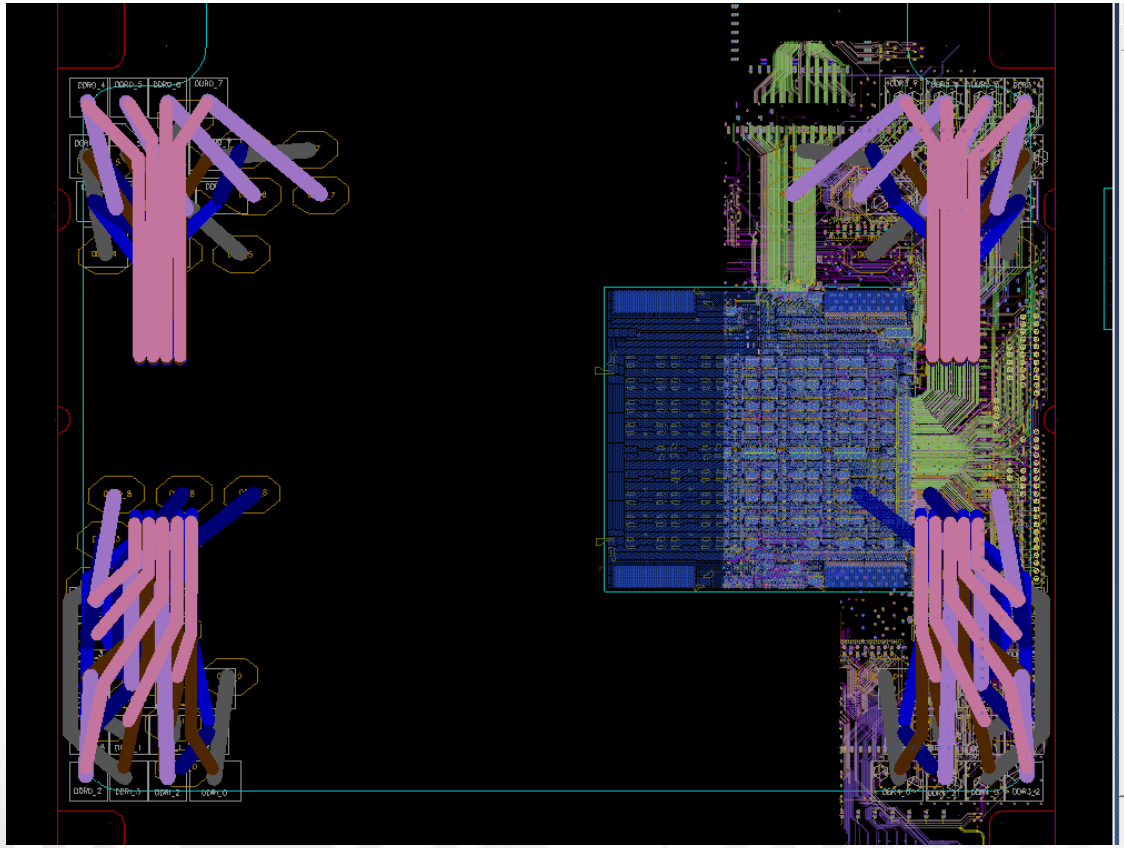
What are the problems with planning of DDR routing

- Planning of DDR routing from Package die to PCB Dimms is very time consuming.
- Many iterations may happen during pathfinding and beyond
- Routing of nets can be a challenge if placement of via farms and LGA pins is not optimal
- Routing proximity of byte lanes to each other is not preferred on back side (after core layers) routing (HLDRC)

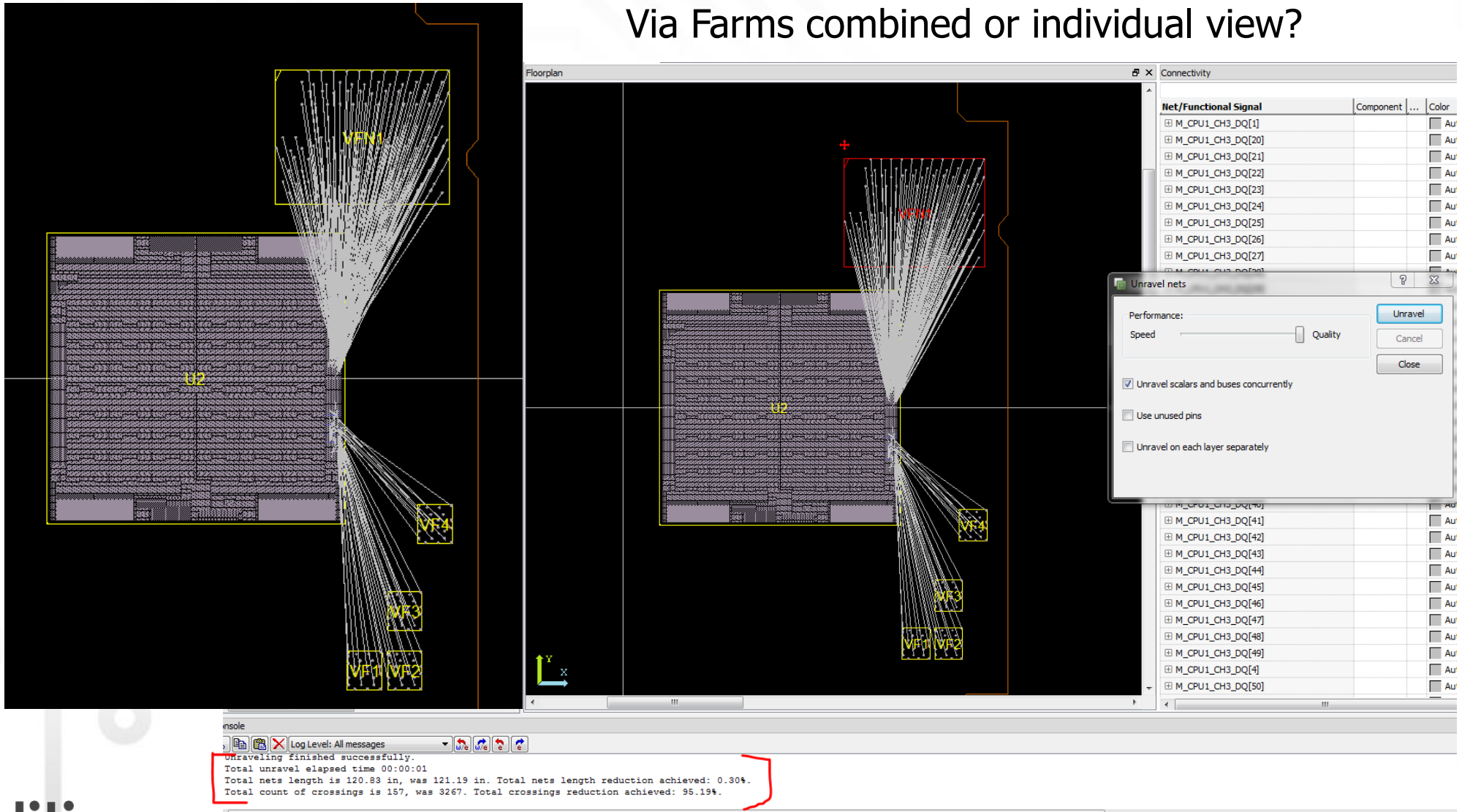
Current manual method of DDR Route planning using user layer graphics to determine layer and byte lane planning used on KNH





Unravel of via farms north before and after unravel

Via Farms combined or individual view?



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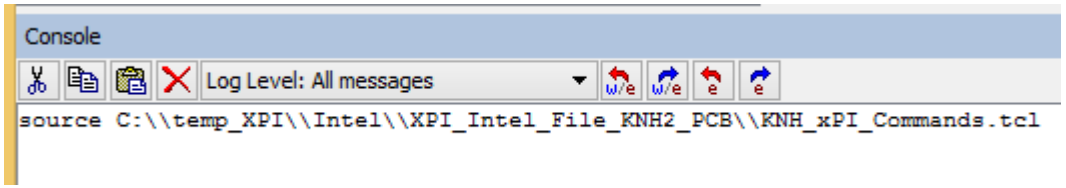
Process for creating and configuring the PCB and Package

- Generate symbol pin list from native CAD tool to create parts
  - Simplifies traditional board translation
- Import text file into XPI when adding part(s)
  - One spreadsheet with more data is good
  - Automation is useful when creating parts
  - Create via farm with multiple ILNs
  - Set swap regions
  - Setting pin groups and colors is helpful

TCL Script for adding PCB database using symbol pin list generated from PCB Layout

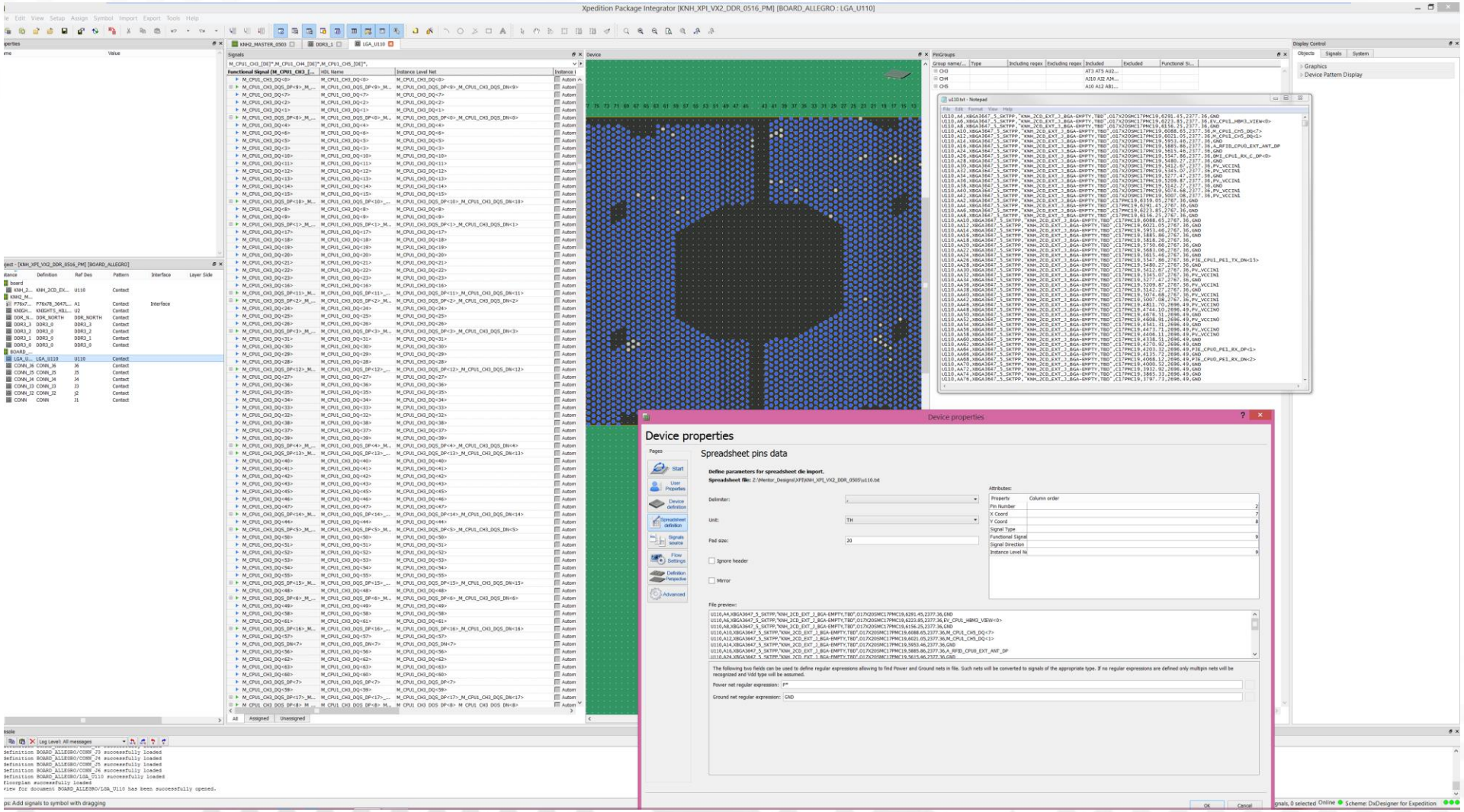
This set of files need to be unzipped in the directory C:\temp_XPI\Intel. Then you can open XPI and run the following command in the console (close the initial create/open dialog form).
source C:\\temp_XPI\\Intel\\XPI_Intel_File_KNH2_PCB\\KNH_xPI_Commands.tcl



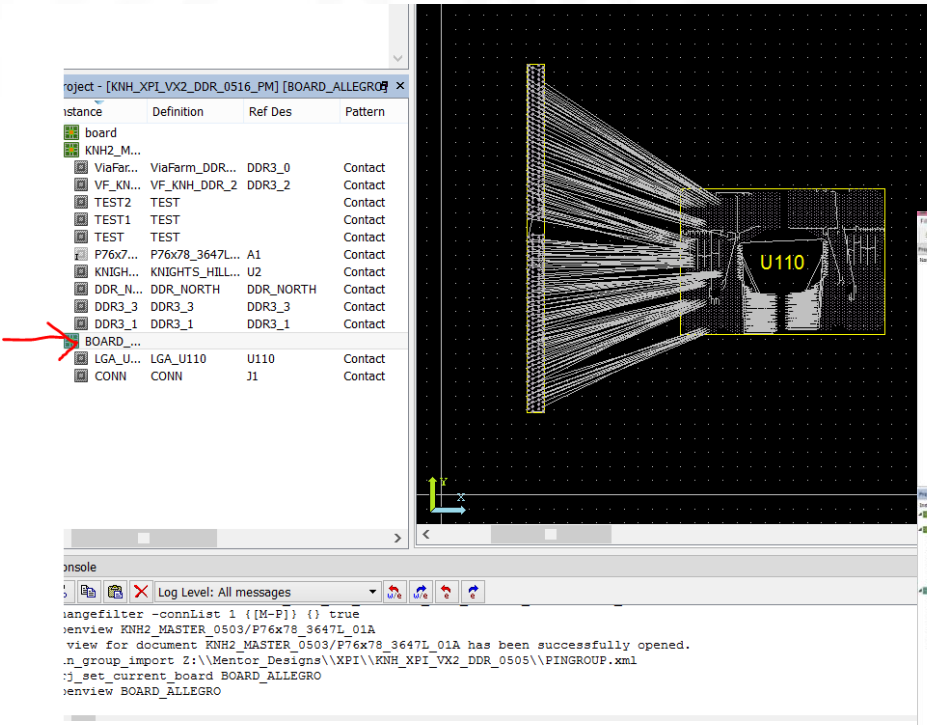
This will open a new KNH project. **Adding the Design PCB**. Read the KNH BGA and Conn288 devices and signal files. It finishes by doing Sync FE Design. At this point the script is done.
These are the steps I did to complete the design and sync the layout.

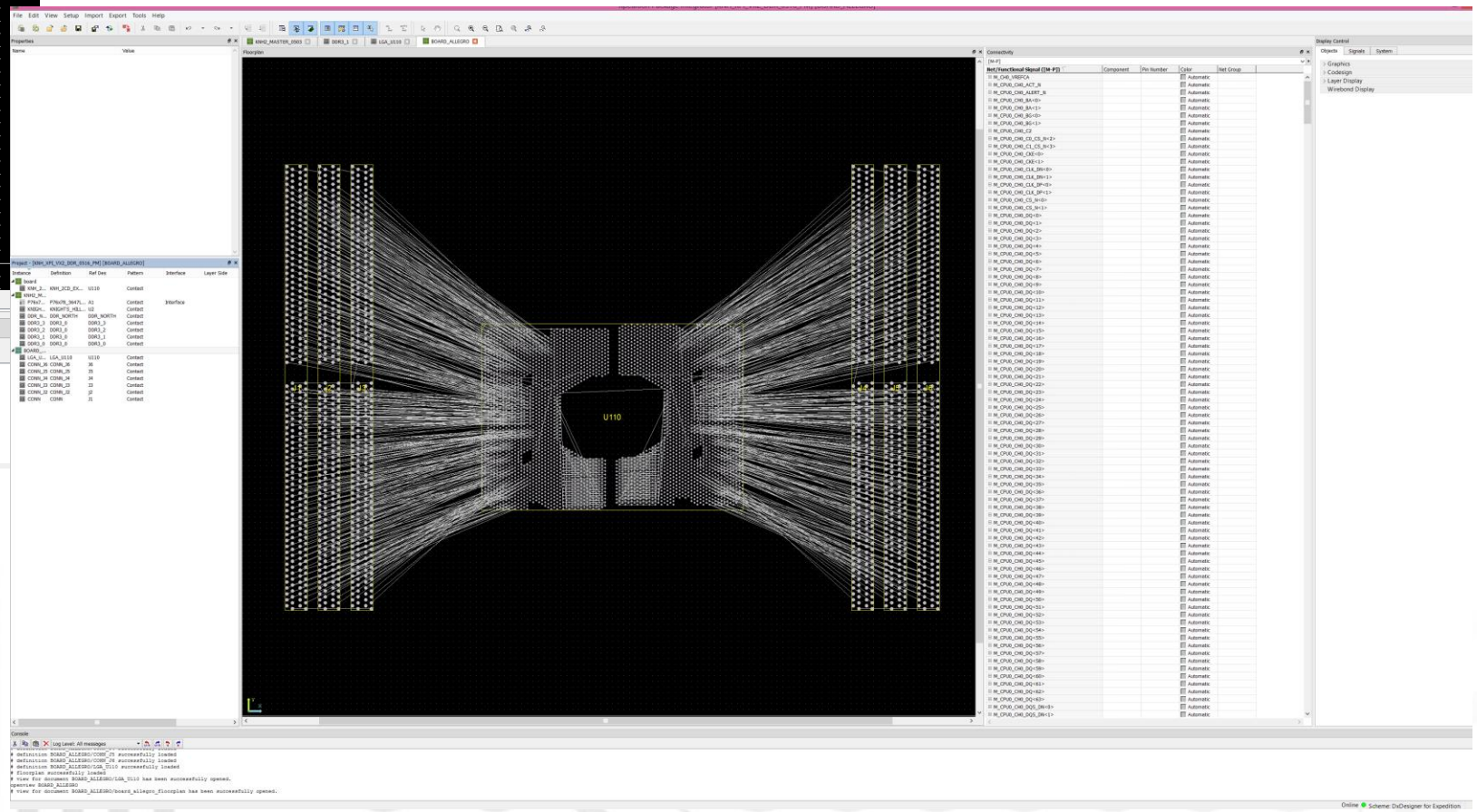
- Select Device KNH_BGA and run Edit >Buses > Autodetect Buses
- Select Device CONN288_J1 and run Edit >Buses > Autodetect BusesSelect Design PCB and run Export > Connectivity to Layout (this will invoke the layout tool
    1. Select the PCB.prj file. Form Next
    2. Design Technology: Package, Template: Package Design 8 Layer Template. Form Finish then Close
    3. Xpedition will Invoke
    4. Copy the C:\temp_XPI\Intel\XPI_Intel_File_KNH2_PCB \place.txt file into directory C:\temp_XPI\Intel\KNH\PCB\PCB
    5. Run FA
    6. Run keyin “pr –file=place.txt”
    7. Grow the Board Outline and Route Border
    8. Save design and exit Xpedition
- In xPI run Import > Layout

Results of TCL Script to build PCB Database

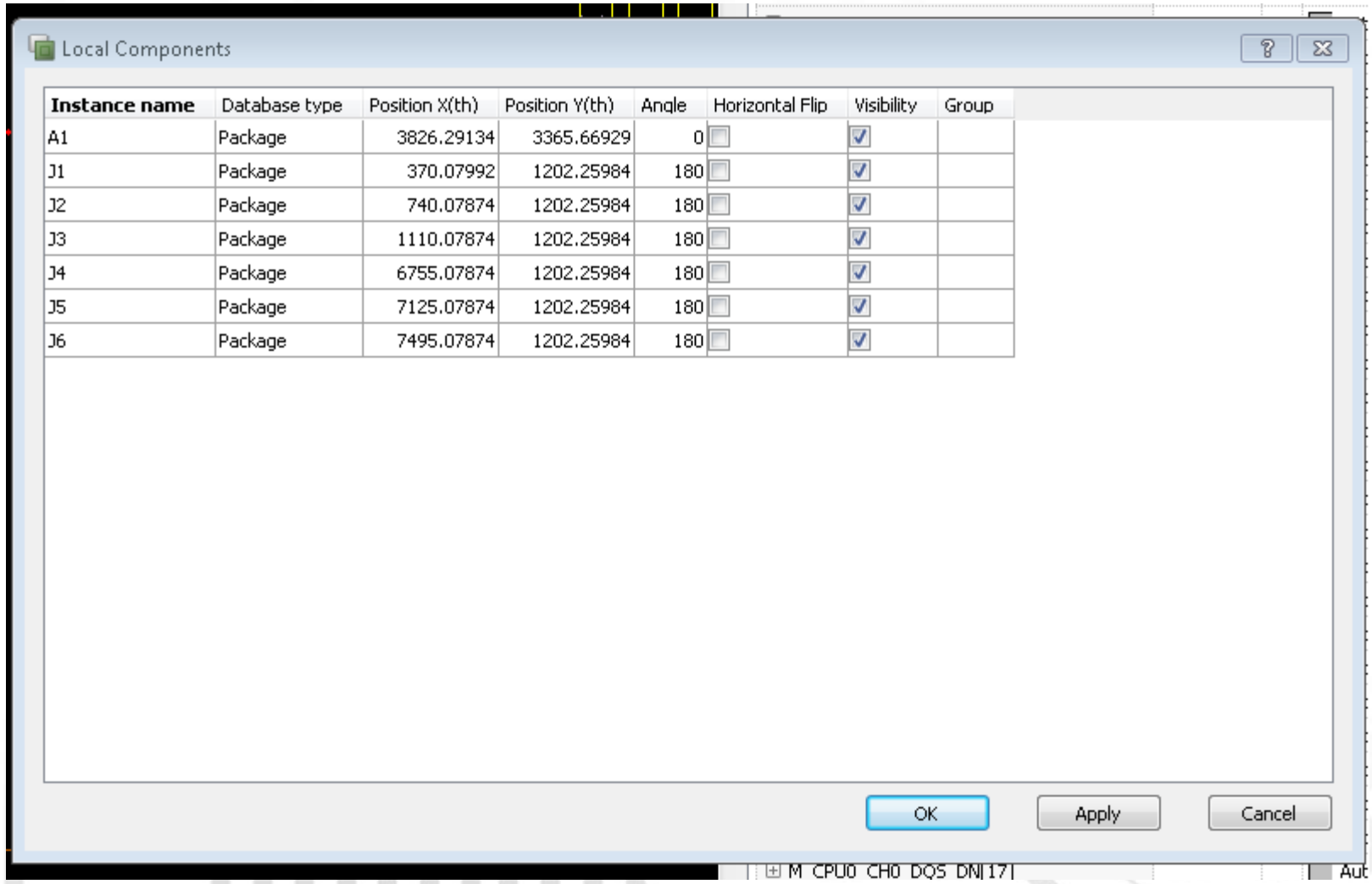


Results of TCL Script to build PCB Database

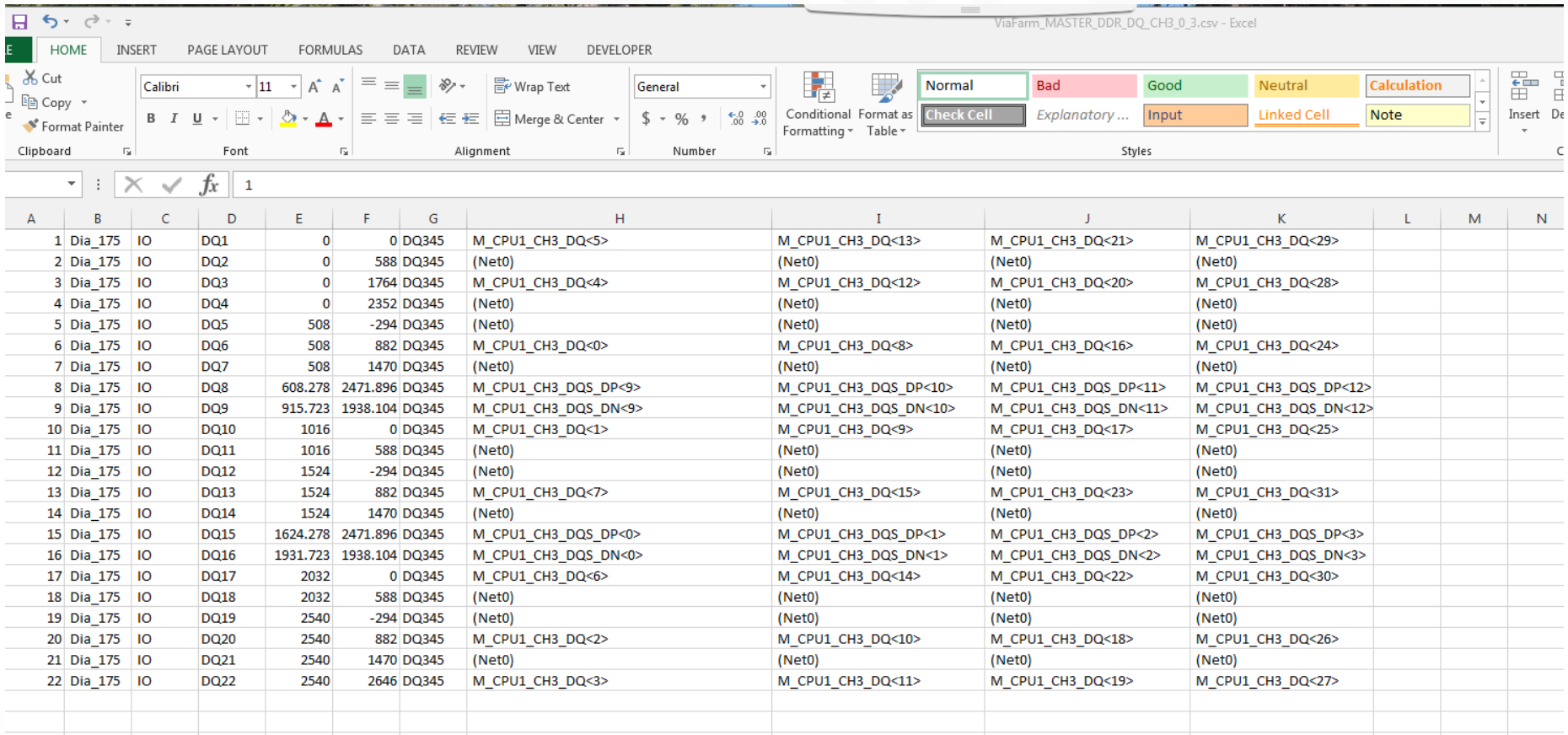




PCB Parts



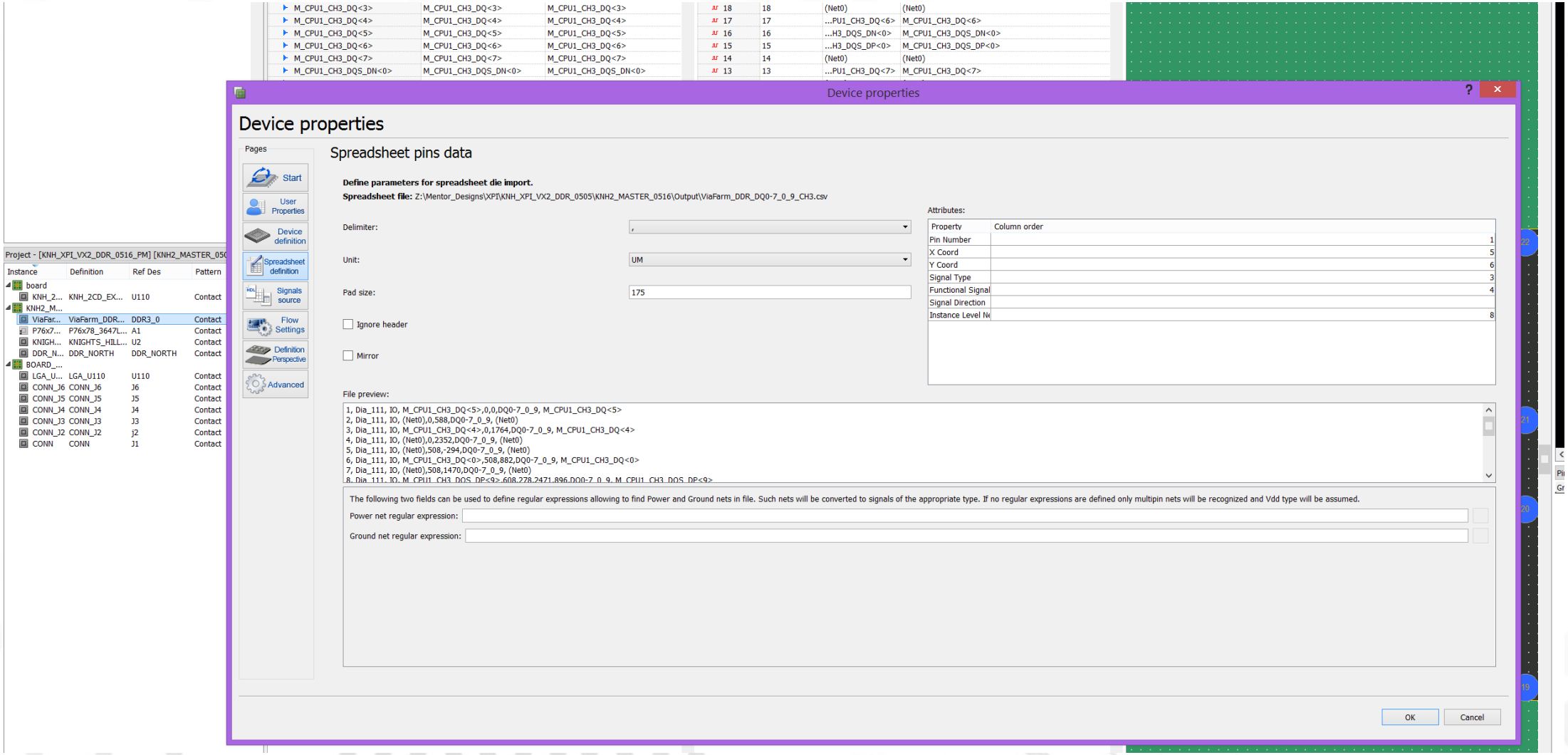
Core Via Farm(s) with ILN's attached to multiple Instances



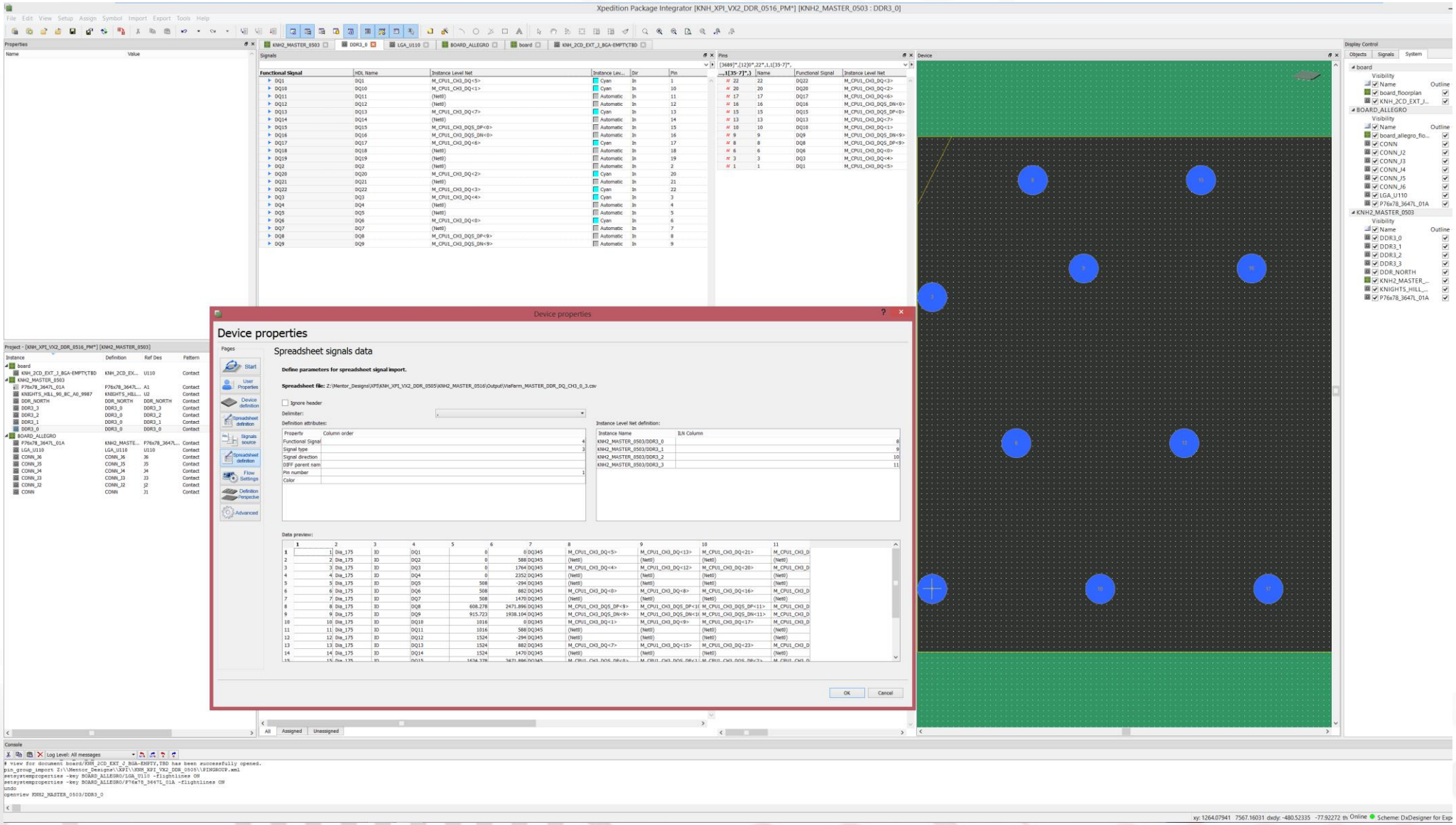
	A	B	C	D	E	F	G	H	I	J	K	L	M	N
1		Dia_175	IO	DQ1	0	0	DQ345	M_CPU1_CH3_DQ<5>	M_CPU1_CH3_DQ<13>	M_CPU1_CH3_DQ<21>	M_CPU1_CH3_DQ<29>			
2		Dia_175	IO	DQ2	0	588	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
3		Dia_175	IO	DQ3	0	1764	DQ345	M_CPU1_CH3_DQ<4>	M_CPU1_CH3_DQ<12>	M_CPU1_CH3_DQ<20>	M_CPU1_CH3_DQ<28>			
4		Dia_175	IO	DQ4	0	2352	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
5		Dia_175	IO	DQ5	508	-294	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
6		Dia_175	IO	DQ6	508	882	DQ345	M_CPU1_CH3_DQ<0>	M_CPU1_CH3_DQ<8>	M_CPU1_CH3_DQ<16>	M_CPU1_CH3_DQ<24>			
7		Dia_175	IO	DQ7	508	1470	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
8		Dia_175	IO	DQ8	608.278	2471.896	DQ345	M_CPU1_CH3_DQS_DP<9>	M_CPU1_CH3_DQS_DP<10>	M_CPU1_CH3_DQS_DP<11>	M_CPU1_CH3_DQS_DP<12>			
9		Dia_175	IO	DQ9	915.723	1938.104	DQ345	M_CPU1_CH3_DQS_DN<9>	M_CPU1_CH3_DQS_DN<10>	M_CPU1_CH3_DQS_DN<11>	M_CPU1_CH3_DQS_DN<12>			
10		Dia_175	IO	DQ10	1016	0	DQ345	M_CPU1_CH3_DQ<1>	M_CPU1_CH3_DQ<9>	M_CPU1_CH3_DQ<17>	M_CPU1_CH3_DQ<25>			
11		Dia_175	IO	DQ11	1016	588	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
12		Dia_175	IO	DQ12	1524	-294	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
13		Dia_175	IO	DQ13	1524	882	DQ345	M_CPU1_CH3_DQ<7>	M_CPU1_CH3_DQ<15>	M_CPU1_CH3_DQ<23>	M_CPU1_CH3_DQ<31>			
14		Dia_175	IO	DQ14	1524	1470	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
15		Dia_175	IO	DQ15	1624.278	2471.896	DQ345	M_CPU1_CH3_DQS_DP<0>	M_CPU1_CH3_DQS_DP<1>	M_CPU1_CH3_DQS_DP<2>	M_CPU1_CH3_DQS_DP<3>			
16		Dia_175	IO	DQ16	1931.723	1938.104	DQ345	M_CPU1_CH3_DQS_DN<0>	M_CPU1_CH3_DQS_DN<1>	M_CPU1_CH3_DQS_DN<2>	M_CPU1_CH3_DQS_DN<3>			
17		Dia_175	IO	DQ17	2032	0	DQ345	M_CPU1_CH3_DQ<6>	M_CPU1_CH3_DQ<14>	M_CPU1_CH3_DQ<22>	M_CPU1_CH3_DQ<30>			
18		Dia_175	IO	DQ18	2032	588	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
19		Dia_175	IO	DQ19	2540	-294	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
20		Dia_175	IO	DQ20	2540	882	DQ345	M_CPU1_CH3_DQ<2>	M_CPU1_CH3_DQ<10>	M_CPU1_CH3_DQ<18>	M_CPU1_CH3_DQ<26>			
21		Dia_175	IO	DQ21	2540	1470	DQ345	(Net0)	(Net0)	(Net0)	(Net0)			
22		Dia_175	IO	DQ22	2540	2646	DQ345	M_CPU1_CH3_DQ<3>	M_CPU1_CH3_DQ<11>	M_CPU1_CH3_DQ<19>	M_CPU1_CH3_DQ<27>			

Could change IO to diff pair parent name, and include color, *possible swap code ILNs** in this spreadsheet. Using one spreadsheet for both part creation and/or signal source would be useful. Also, the ability to use multiple ILN would be good when building part if possible.

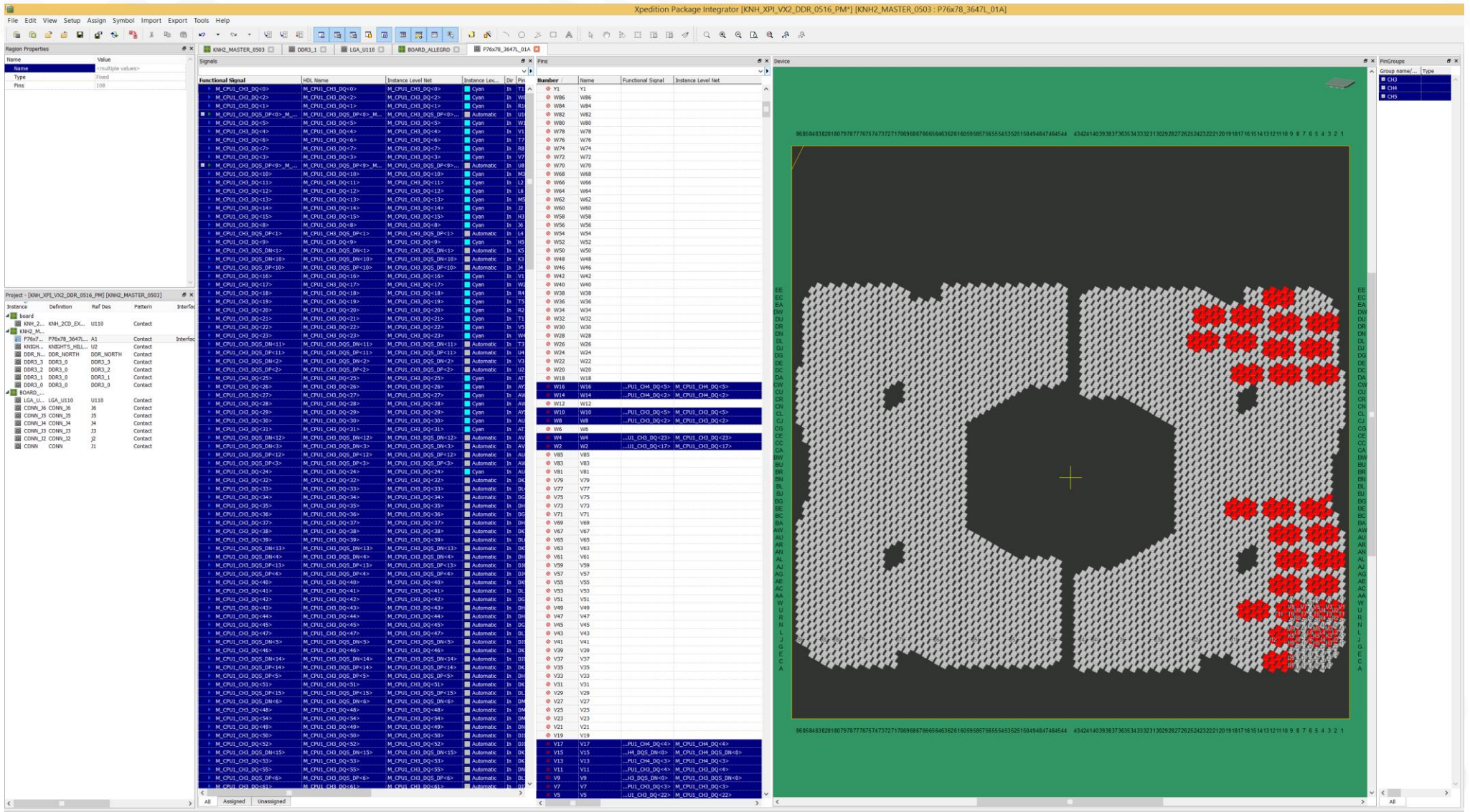
Building Via Farms



Multiple ILN's for multiple instances



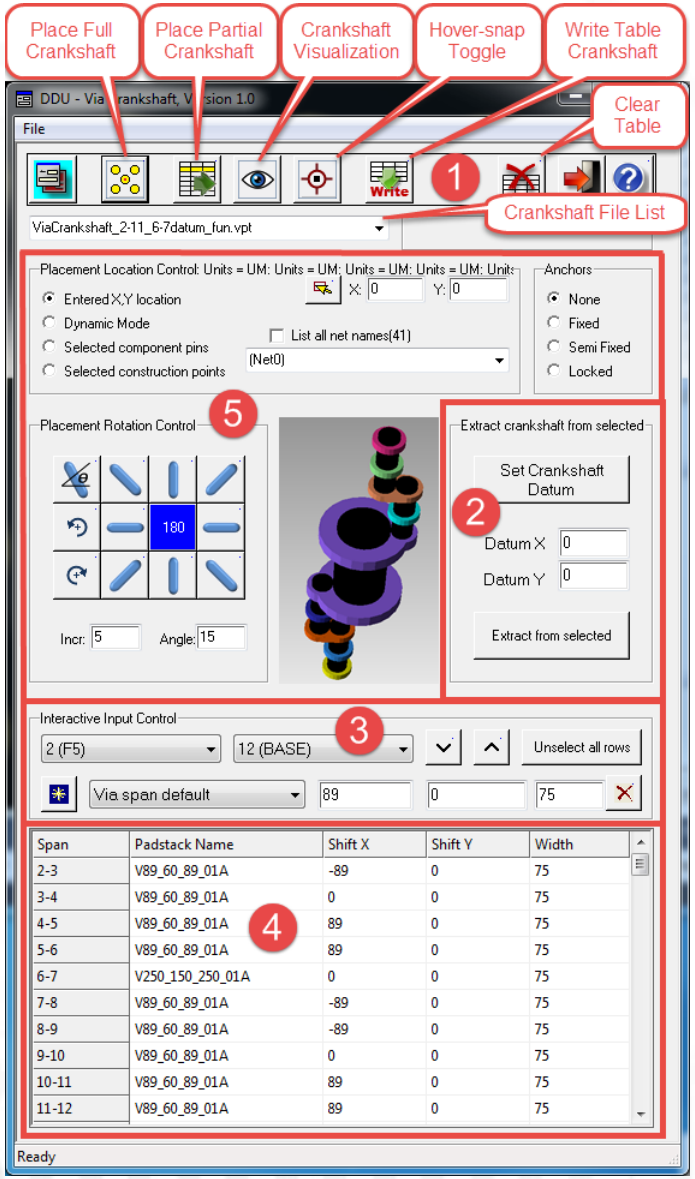
Defining DDR BYTE Lane pin groups



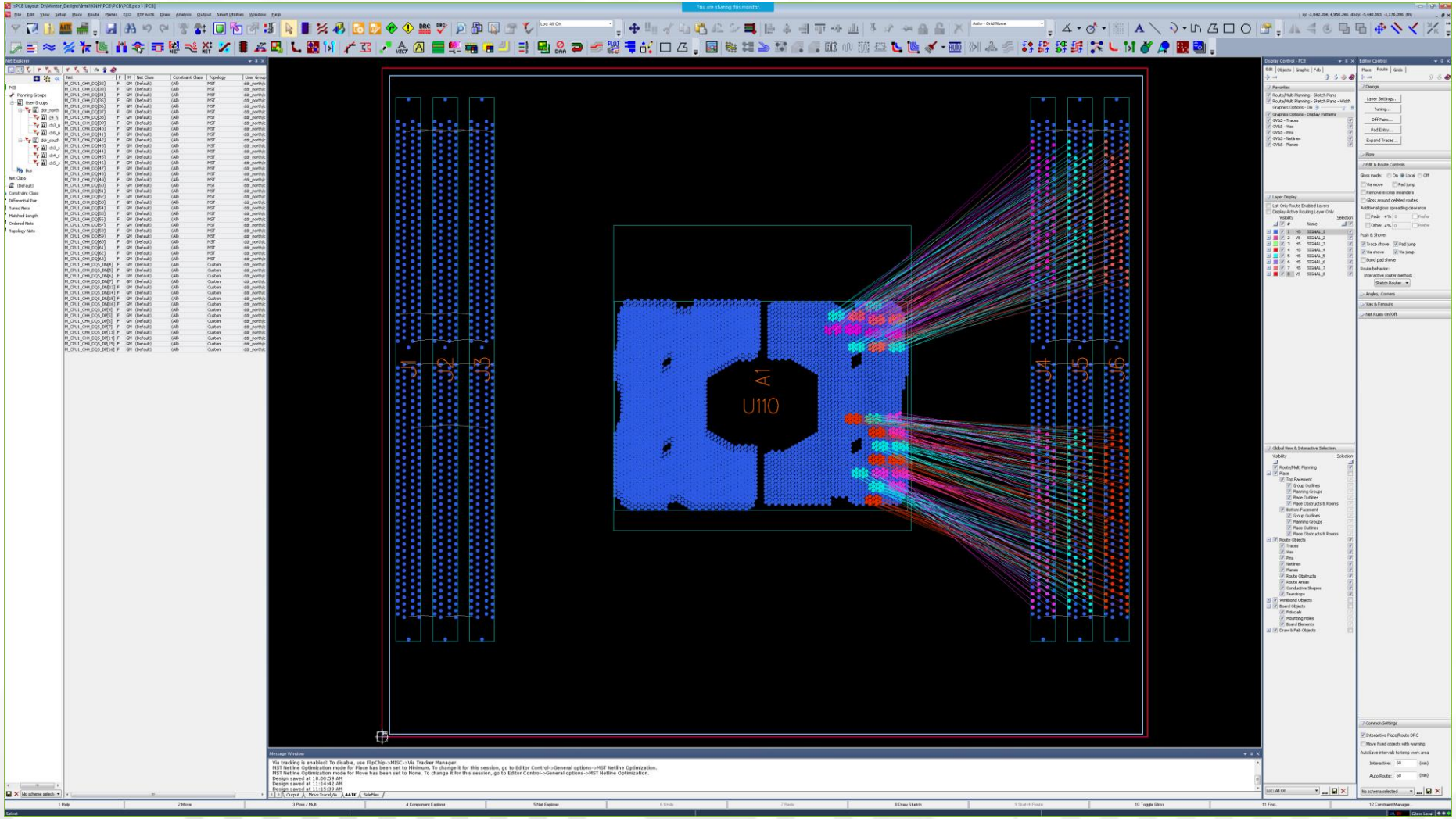
Assign Crankshaft Vias on Via Farms

Create and assign via crankshafts with net adoption from selected pins or existing net objects in added crankshaft via location.

1. Via crankshaft toolbar and file control
2. Extract via crankshaft from selected
3. Interactive build via crankshaft
4. Via crankshaft Table
5. Dynamic and menu placement control



PCB with package LGA and Board LGA View per Byte lane



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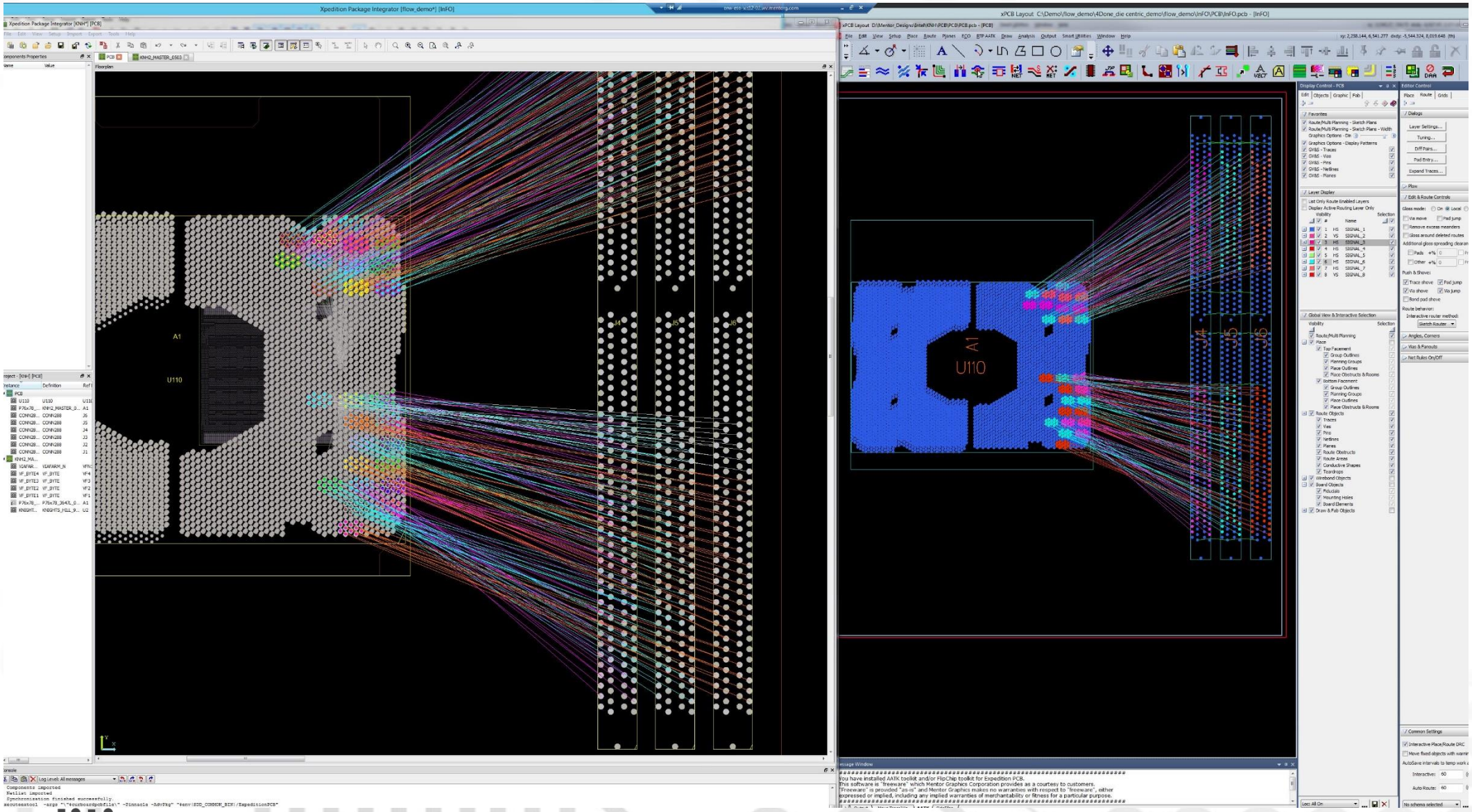
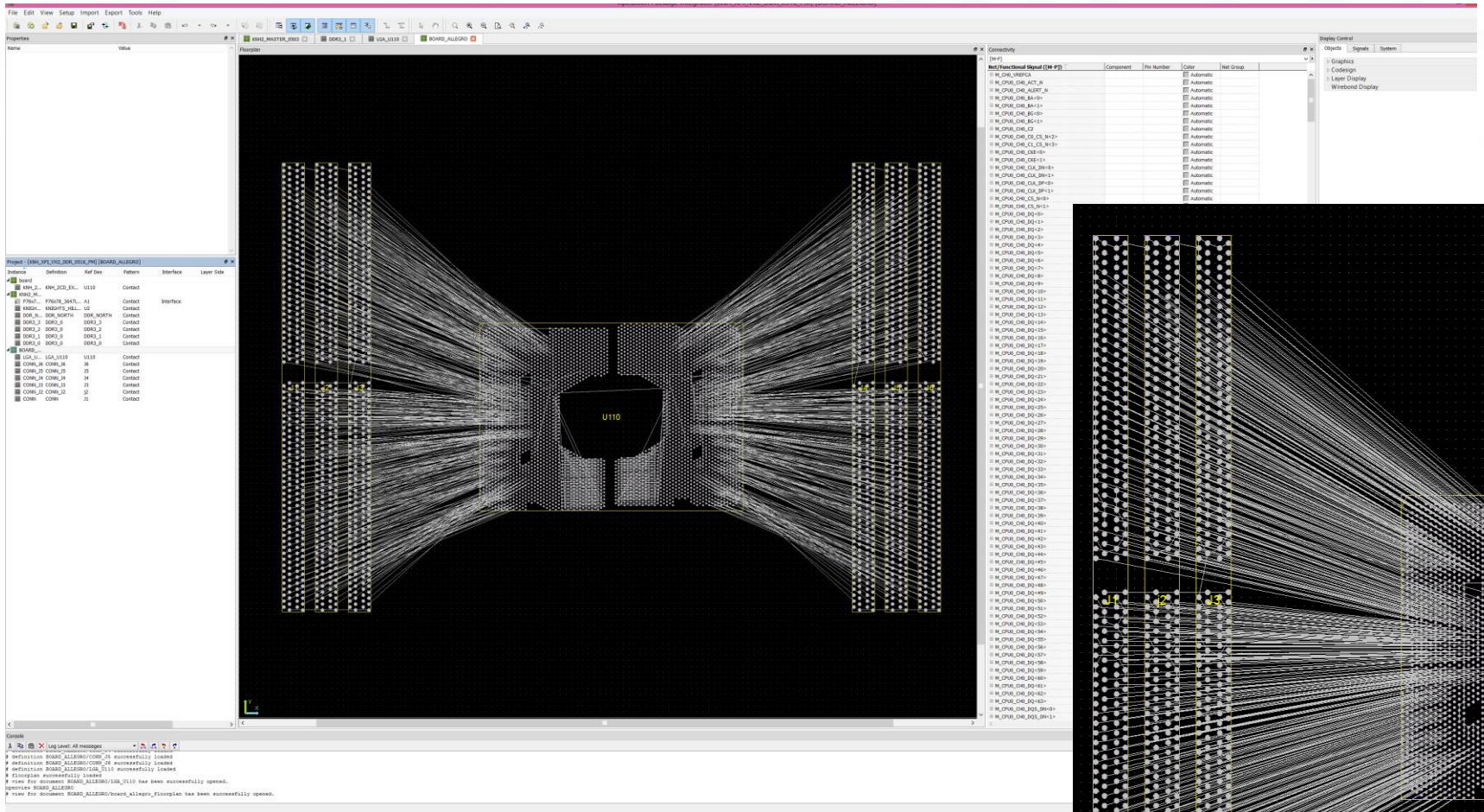
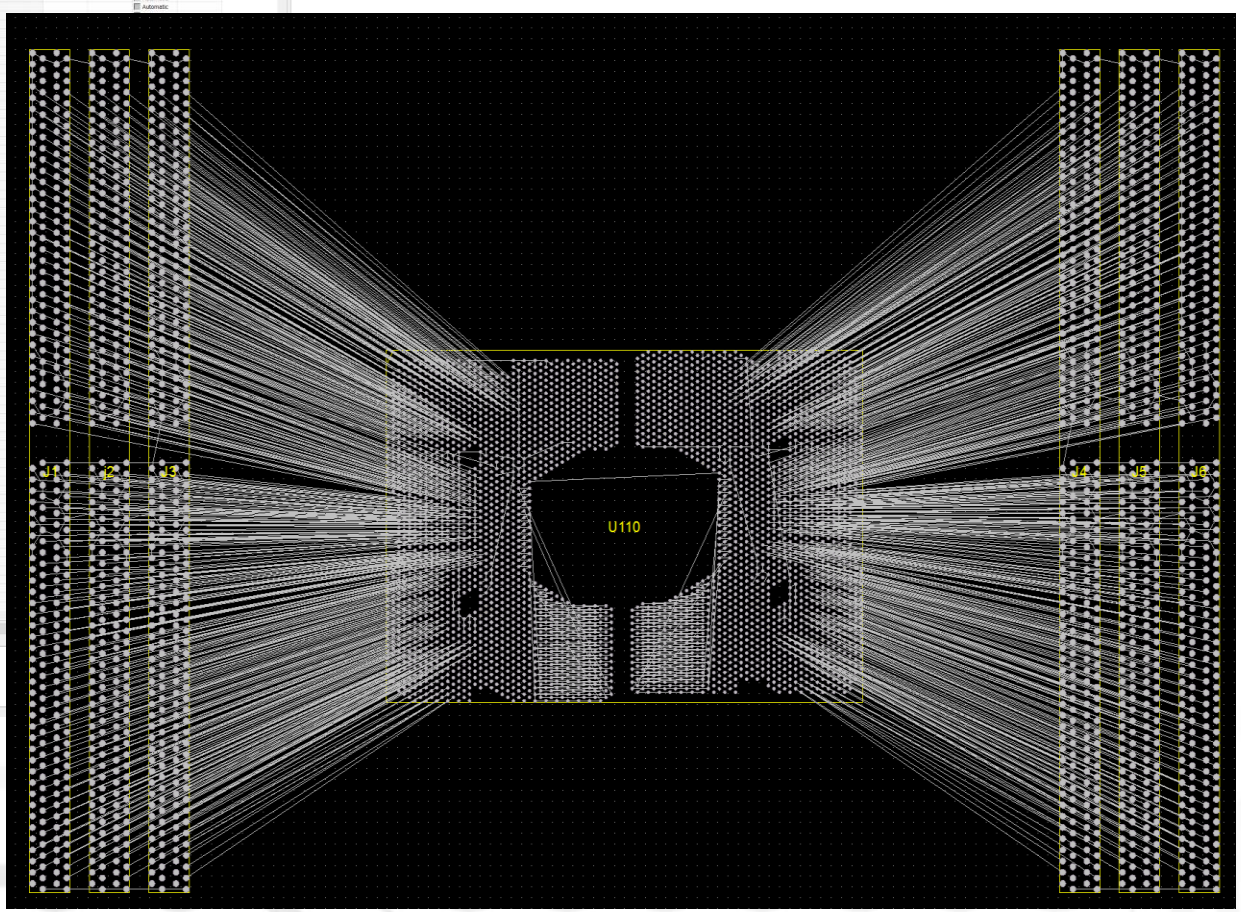
Die and PCB Floorplan in Floorplan XPI view and PCB View



PCB Before and After Unravel





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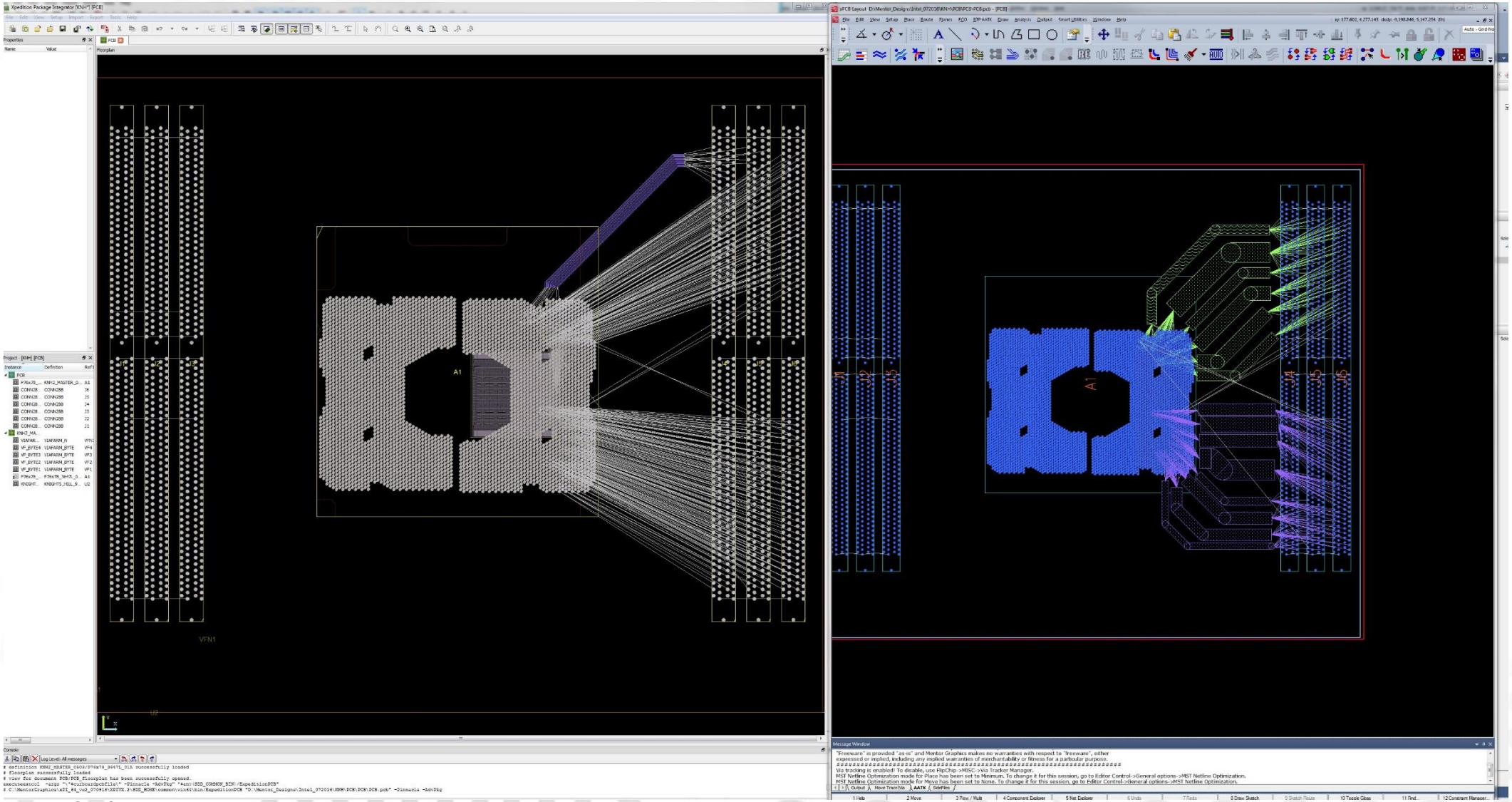
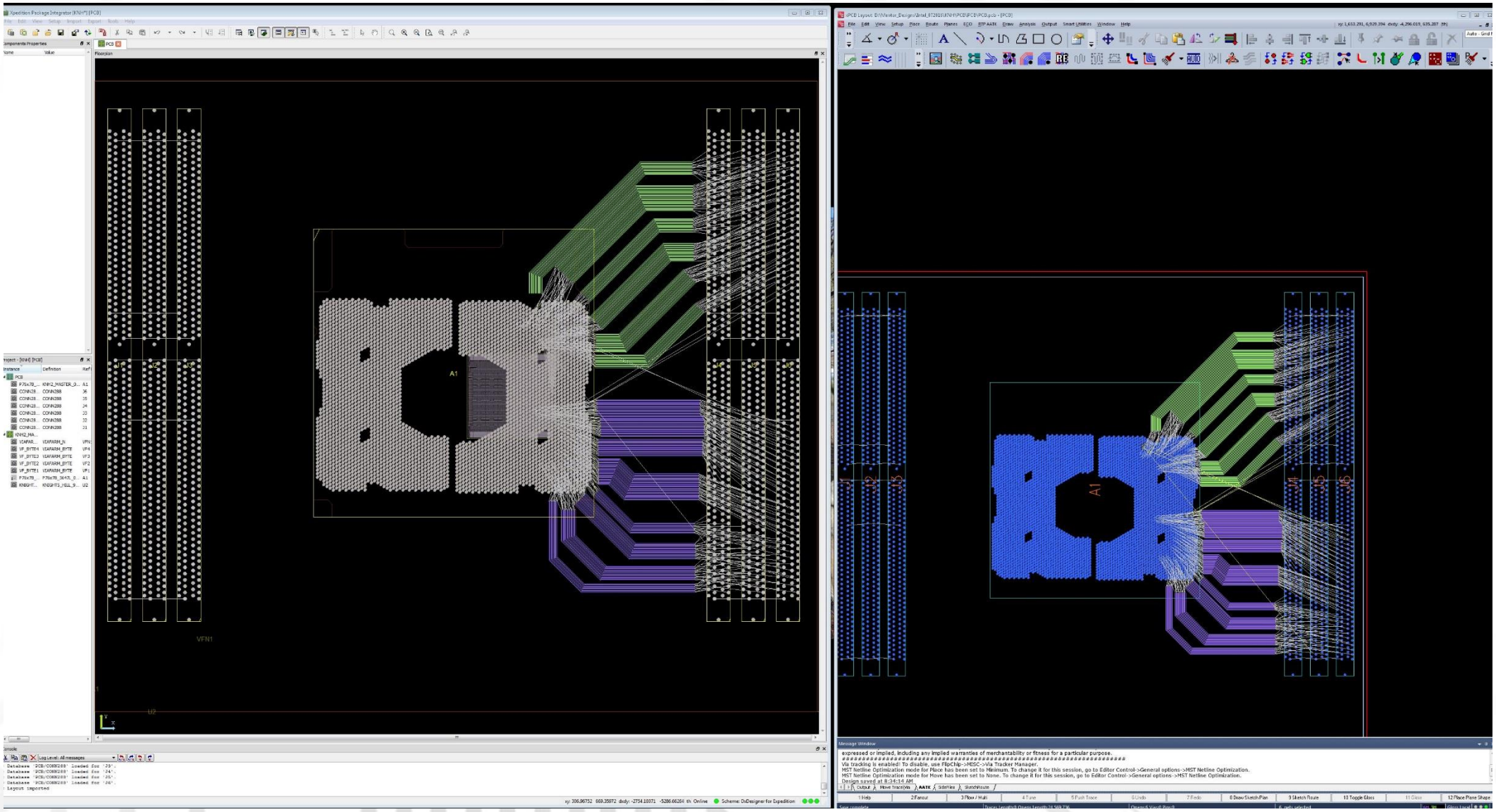
xPI and xPCB Sketch Planner view



PCB view with Package Floor plan with trunk routing



Package Integrator Demo

Sketch Router/Planner/Trunk routing demo